Correlation between the electrical properties of p-Si/n-4H-SiC junctions and concentrations of acceptors in Si

2015 Jpn. J. Appl. Phys. 54 030210

(http://iopscience.iop.org/1347-4065/54/3/030210)

Correlation between the electrical properties of p-Si/n-4H-SiC junctions and concentrations of acceptors in Si

Shota Nishida[1], Jianbo Liang[1], Tomohiro Hayashi[1], Manabu Arai[2], and Naoteru Shigekawa[1*]

[1]*Graduate School of Engineering, Osaka City University, Osaka 558-8585, Japan*
[2]*New Japan Radio Co., Ltd., Chuo, Tokyo 103-8456, Japan*
E-mail: shigekawa@elec.eng.osaka-cu.ac.jp

Received August 1, 2014; revised September 16, 2014; accepted September 29, 2014; published online January 16, 2015

We fabricated p^+-, p-, and p^--Si/n-4H-SiC junctions by surface activated bonding (SAB). We investigated their electrical properties by measuring their current–voltage (*I–V*) characteristics at raised ambient temperatures, capacitance–voltage (*C–V*) characteristics at various frequencies, and capacitance–frequency (*C–f*) characteristics at room temperature. The activation energy of their reverse-bias current and the flat-band voltage in their *C–V* characteristics, which were estimated to be 0.97–1.01 eV and 0.83–0.84 V, respectively, were insensitive to the concentrations of acceptors in Si substrates. The relaxation times estimated from the *C–f* characteristics were 0.8 and 1.5 μs for the p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions, respectively. The results are explained by a scheme wherein Fermi level pinning occurs at the Si/4H-SiC interfaces fabricated by SAB.

1. Introduction

Recently, owing to its large bandgap and high thermal conductivity, silicon carbide (SiC) has been extensively studied as a promising material for high-power and high-efficiency applications.[1)] SiC-based electron devices such as Schottky barrier diodes and MOSFETs have been intensively investigated, and SiC-based power modules have recently been commercialized.[2,3)] The combination of SiC with Si technologies holds promise for high-frequency, high-power, and high-temperature operating devices, modules, and integrated circuits.[4,5)] Si/SiC junctions are of great potential as constituents of bipolar transistors with large current gains, diodes with high breakdown voltages, and Si/SiC monolithically integrated circuits.[6–8)] the possibility of applying Si/SiC junctions as an intermediate structure for fabricating high-quality SiC MOS devices has been explored.[9,10)] However, the difficulty in fabricating Si/SiC junctions because of the different crystal structures and lattice constants between the two materials has limited the performance of the junctions.[11)]

As an alternative approach to overcoming these difficulties and realizing a variety of heterogeneous structures with high mechanical strength, the direct wafer bonding method has been investigated in recent years.[12,13)] This method has been employed for fabricating various junctions made of semiconductor materials with different crystal structures or lattice constants, such as Si/GaAs,[14)] Si/InGaP,[15)] Si/InP,[16)] Si/GaN,[17)] and Si/SiC.[18)]

Among the various direct bonding methods, we focus on surface activated bonding (SAB), in which samples are bonded to each other after their surfaces are activated by Ar plasma irradiation.[19–21)] We previously fabricated Si/SiC junctions and investigated their physical and electrical properties and the effects of thermal annealing.[22,23)]

In this work, we fabricated p^+-, p-, and p^--Si/n-4H-SiC junctions by SAB and examined the correlation between their electrical properties and the concentration of acceptors in Si. The electrical properties of the respective junctions were investigated by measuring their current–voltage (*I–V*) characteristics at raised ambient temperatures, and their capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) characteristics at room temperature. We estimated the activation energy of reverse-bias current, the flat-band voltage, and the relaxation time in these junctions.

Table I. Carrier concentrations of bonded p-Si substrates and estimated activation energies, flat-band voltages, and relaxation times of the junctions.

	p^+-Si/n-4H-SiC	p-Si/n-4H-SiC	p^--Si/n-4H-SiC
N_A (cm^{-3})	2.6×10^{19}	2.4×10^{17}	1.4×10^{15}
E_a (eV)	1.01	0.97	0.98
V_b (V)	0.84	0.83	0.84
τ (μs)	—	0.8	1.5

2. Experimental procedure and results

2.1 Sample preparation

We employed B-doped (100) p^+-, p-, and p^--Si substrates and an n-4H-SiC layer epitaxially grown on n^+-4H-SiC substrates. The Hall measurements at room temperature revealed that the carrier concentrations of Si substrates were 2.6×10^{19} (p^+-Si), 2.4×10^{17} (p-Si), and 1.4×10^{15} cm^{-3} (p^--Si), respectively. These values are shown in Table I. The *C–V* measurement of n-4H-SiC Schottky diodes at room temperature and a frequency of 100 kHz revealed that the carrier concentration in n-4H-SiC epitaxial layers (6 μm) was 5.5×10^{15} cm^{-3}. The nominal carrier concentrations in buffer layers (0.5 μm) and n^+-4H-SiC substrates (360 μm) were $>1 \times 10^{18}$ (buffer layers) and $\sim 3 \times 10^{18}$ cm^{-3} (substrates).

Before junctions were fabricated, we formed Al/Ni/Au multilayer metal contacts on n^+-4H-SiC substrates by vacuum evaporation followed by annealing at 1000 °C for 60 s in N_2 gas ambient to obtain good ohmic contacts for n-4H-SiC. The 4H-SiC epitaxial substrates and three types of Si substrates (p^+-, p-, and p^--Si substrates) were bonded to each other. The bonded samples were annealed at 700 °C for 60 s to improve the mechanical strength and electrical properties.[23)] Then, Al contacts were evaporated to p-Si substrates, by annealing at 400 °C for 60 s, ohmic contacts were achieved. We diced the respective junctions into 1.7×1.7 mm^2 chips with metallization of their tops and bottoms. We measured the *I–V* characteristics at raised ambient temperature using an Agilent B2902A and the *C–V* and *C–f* characteristics at room temperature using an Agilent E4980A.

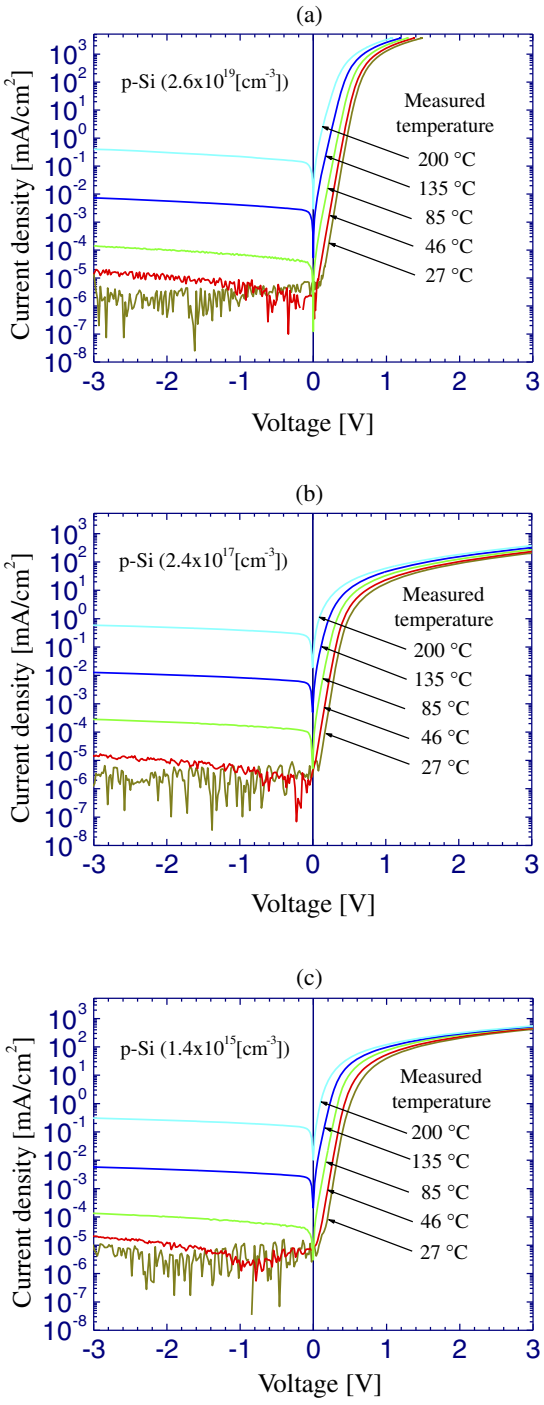

Fig. 1. (Color online) *I–V* characteristics of (a) p^+-Si/n-4H-SiC, (b) p-Si/n-4H-SiC, and (c) p^--Si/n-4H-SiC junctions measured at various temperatures.

2.2 Current–voltage characteristics

The *I–V* characteristics of p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions measured at temperatures between 27 and 200 °C are shown in Figs. 1(a)–1(c), respectively. The *I–V* characteristics of the three junctions show rectifying properties at both temperatures. The magnitudes of the currents for reverse-bias voltages of these junctions are equal to each other at each temperature. It is notable that the magnitude of the reverse-bias currents measured at 27 °C is lower than those previously measured at room temperature for n-Si/n-SiC[8] and p-Si/n-SiC[24] junctions fabricated by

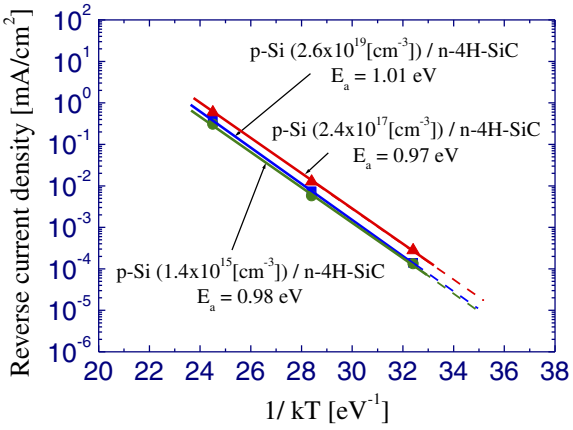

Fig. 2. (Color online) Dependence of the reverse-bias current measured at −3 V on the ambient temperature for p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions.

other methods. The reverse-bias current increases by $\sim 10^5$ times as the measurement temperature increases to 200 °C. We also find that the slope of the currents obtained at 85, 135, and 200 °C for reverse-bias voltages between −1 and −3 V does not vary as the measurement temperature increases. The relationship between the reverse-bias current at −3 V and the measurement temperature is shown in Fig. 2. The data obtained at 27 and 46 °C are not shown in this figure because they are below the measurement resolution. The dependence of reverse-bias current on temperature is approximately expressed as $I \propto \exp(-E_a/kT)$, where E_a is the activation energy.[23,25] We estimate E_a to be 1.01, 0.97, and 0.98 eV for the p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions, respectively. These E_a values are summarized in Table I. We find that these values are larger than E_a of the p-Si/n-4H-SiC junctions without annealing (0.33 eV).[23]

2.3 Capacitance–voltage characteristics

C–V measurements were performed at frequencies ranging from 1 kHz to 1 MHz at room temperature. The $1/C^2$–*V* characteristics of p^+-, p-, and p^--Si/n-4H-SiC junctions are shown in Figs. 3(a)–3(c), respectively. As is shown in Fig. 3(a), $1/C^2$ is insensitive to frequency and almost linearly depends on bias voltage. In contrast, as is seen from Figs. 3(b) and 3(c), marked warps and frequency dispersion are observed at frequencies higher than 50 kHz in the p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions. Their $1/C^2$–*V* characteristics measured at frequencies between 1 and 10 kHz are linear and in agreement with each other. By linearly extrapolating $1/C^2$ of the respective junctions at 10 kHz to zero, we extracted the flat-band voltages (V_b) of 0.83, 0.84, and 0.83 V for p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions, respectively. These V_b values are shown in Table I. It is notable that these values are in agreement with each other.

The *C–f* characteristics of p- and p^--Si/n-4H-SiC junctions, whose $1/C^2$–*V* characteristics revealed a marked frequency dispersion, were measured at 0 V and room temperature. The frequencies of measurements ranged from 1 kHz to 2 MHz. The results are shown in Fig. 4. In each junction, the capacitance remains almost constant for frequencies lower than 10 kHz and higher than 1 MHz, whereas it drastically decreases as the frequency increases from 10 kHz to 1 MHz.

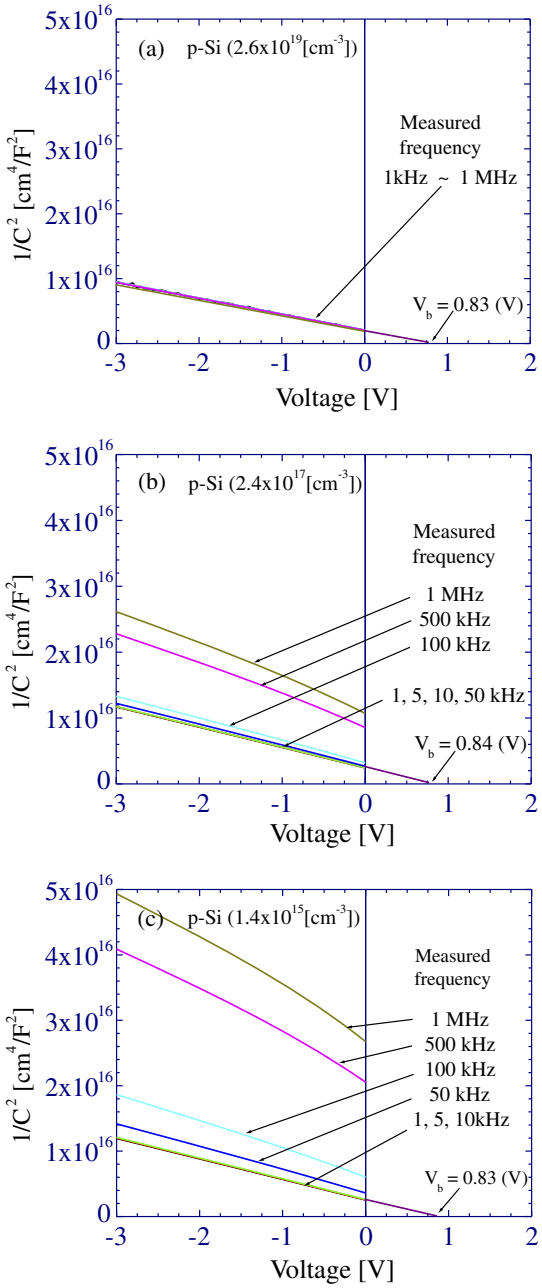

Fig. 3. (Color online) C–V characteristics of (a) p^+-Si/n-4H-SiC, (b) p-Si/n-4H-SiC, and (c) p^--Si/n-4H-SiC junctions measured at room temperature and frequencies ranging from 1 kHz to 1 MHz.

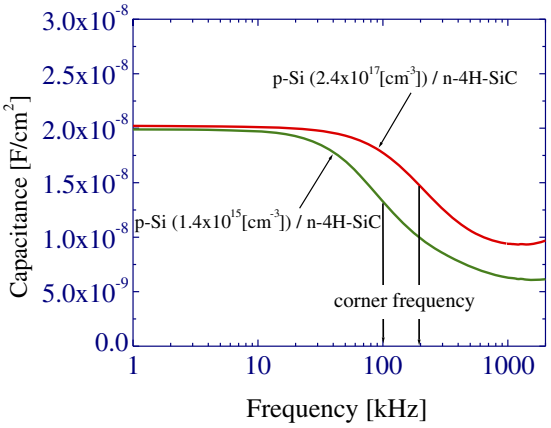

Fig. 4. (Color online) C–f characteristics of p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions measured at room temperature and frequencies ranging from 1 kHz to 2 MHz.

The corner frequencies, or the frequencies that give a capacitance corresponding to the average of its low- and high-frequency limits, $(C_{lf} + C_{hf})/2$, which likely characterize the variation in capacitance in this frequency range,[26] are 195 and 105 kHz in the p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions, respectively. The relaxation times defined as $1/(2\pi \times \text{corner frequency})$[26] are 0.8 and 1.5 μs for the p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions, respectively. The relaxation times of the two junctions are given in Table I.

3. Discussion

The result that the C–V characteristics measured for frequencies lower than 10 kHz and the flat band voltages of p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions are similar to each other suggests that the depletion layer formed in the SiC substrate only contributes to the capacitance, i.e., the junctions behave as one-sided junctions, in this frequency region. We extracted the concentration of dopants from the $1/C^2$–V characteristics at 10 kHz in this framework. It is notable that the obtained concentrations, $(3.1–4.7) \times 10^{15}\,\text{cm}^{-3}$ in the three junctions, are close to the nominal concentration of donors in the SiC bonding layer.

It is assumed that for lower frequencies the interface states of Si/SiC junctions are charged and/or discharged in response to the bias voltage change so that the electrical charges at the interface, or the carriers trapped at the interface states, are in equilibrium with those in the Si layers. Given that the response of the charges at the interface depends on the tunneling of electrons between the valence band of Si substrates and the interface states across the depletion layer of Si, a delay should occur so that the depletion layer thickness in the Si substrates should be modulated in the case of measurements at high frequencies. The delay in the response is likely more marked in junctions with Si substrates with lower doping concentrations. The observed frequency dispersion in the capacitances of p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions [Figs. 3(b) and 3(c)] and the longer relaxation time deduced from the C–f characteristics of the p^--Si/n-4H-SiC junction (Fig. 4) can be explained in this scheme. The result that $V_b \approx 0.83–0.84$ V suggests that in the low-frequency ($\leq$10 kHz) measurements, the Fermi level seems to be pinned at an energy $qV_b - \delta_n \approx 1.05$ eV below the conduction band edge of the SiC layer at the interface. The band diagram of Si/SiC junctions based on this scheme is schematically shown in Fig. 5.

The observed similarity in the I–V characteristics and E_a among the p^+-Si/n-4H-SiC, p-Si/n-4H-SiC, and p^--Si/n-4H-SiC junctions is consistent with aforementioned scheme that the electrical characteristics of these junctions are dominated by the SiC layers in low-frequency measurements. The result that E_a of 0.97–1.01 eV was obtained suggests that the current for the reverse bias voltages is dominated by (i) the thermal excitation of electrons in the valence band in Si layers to their conduction band and (ii) their subsequent tunneling across the depletion layer in the SiC substrate. The first process in the above scheme might be the excitation of electrons trapped in the interface to states with a high energy

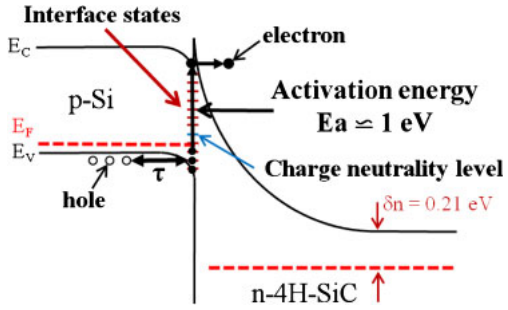

Fig. 5. (Color online) Band diagram and hypothetical process of electron transport across the interface of Si/SiC junctions.

of approximately 1 eV. The hypothetical process of electron transport across the interface is also shown in Fig. 5. Given that the details of the mechanism of electrical conduction across the Si/SiC interfaces are not yet completely understood, the fundamental properties of the Si/SiC interfaces must be investigated in greater depth in order to explore the possibilities of devices made of SAB-based Si/SiC junctions.

4. Conclusions

We fabricated p^+-, p-, and p^--Si/n-4H-SiC junctions by surface activated bonding (SAB) and investigated their electrical properties by measuring current–voltage and capacitance–voltage characteristics. The current–voltage characteristics of the three junctions for reverse-bias voltages at a raised ambient temperature were similar to each other. The activation energies of the reverse-bias current were 0.97–1.01 eV. The flat band voltages of respective junctions deduced from the capacitance–voltage characteristics at 10 kHz were similar to each other (0.83 V: p^+-Si/n-4H-SiC; 0.84 V: p-Si/n-4H-SiC; 0.83 V: p^--Si/n-4H-SiC). The capacitance–frequency characteristics of the p-Si/n-4H-SiC and p^--Si/n-4H-SiC junctions were measured at an applied voltage of 0 V and frequencies ranging from 1 kHz to 2 MHz. The relaxation time extracted from the characteristics is longer in the junctions made of Si substrates with lower concentrations of acceptors (0.8 μs: p-Si/n-4H-SiC and 1.5 μs: p^--Si/n-4H-SiC). These results are explained by a scheme wherein the Fermi level is pinned at the Si/4H-SiC interfaces in low-frequency (typically ≤10 kHz) measurements.

Acknowledgments

Part of this work was supported by the "Creative research for clean energy generation using solar energy" project in Core Research for Evolutional Science and Technology (CREST) programs of the Japan Science and Technology Agency (JST).

1) H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, J. Appl. Phys. **76**, 1363 (1994).
2) M. Yoshimoto, R. Araki, T. Kurumi, and H. Kinoshita, ECS Trans. **50** [7], 61 (2013).
3) Web [http://www.mitsubishielectric.com/news/2013/0509-a.html].
4) T. Hayashi, Y. Shimoida, H. Tanaka, S. Yamagami, S. Tanimoto, and M. Hoshi, Mater. Sci. Forum **527–529**, 1453 (2006).
5) K.-H. Wu, Y.-K. Fang, J.-H. Zhou, and J.-J. Ho, Jpn. J. Appl. Phys. **36**, 5151 (1997).
6) H. Kroemer, Proc. IEEE **70**, 13 (1982).
7) P. H. Yih, J. P. Li, and A. J. Steckl, IEEE Trans. Electron Devices **41**, 281 (1994).
8) A. Pérez-Tomás, M. R. Jennings, M. Davis, J. A. Covington, and P. A. Mawby, J. Appl. Phys. **102**, 014505 (2007).
9) H. Shinohara, H. Kinoshita, and M. Yoshimoto, Appl. Phys. Lett. **93**, 122110 (2008).
10) M. R. Jennings, A. Pérez-Tomás, O. J. Guy, R. Hammond, S. E. Burrows, P. M. Gammon, M. Lodzinski, J. A. Covington, and P. A. Mawby, Electrochem. Solid-State Lett. **11**, H306 (2008).
11) A. N. Nazarov, Ya. N. Vovk, V. S. Lysenko, V. I. Turchanikov, V. A. Scryshevskii, and S. Ashok, J. Appl. Phys. **89**, 4422 (2001).
12) H. Takagi, R. Maeda, T. R. Chung, N. Hosoda, and T. Suga, Jpn. J. Appl. Phys. **37**, 4197 (1998).
13) N. Shigekawa, M. Morimoto, S. Nishida, and J. Liang, Jpn. J. Appl. Phys. **53**, 04ER05 (2014).
14) S. Essig and F. Dimroth, ECS J. Solid State Sci. Technol. **2**, Q178 (2013).
15) J. Liang, M. Morimoto, S. Nishida, and N. Shigekawa, Phys. Status Solidi C **10**, 1644 (2013).
16) H. Wada and T. Kamijoh, Jpn. J. Appl. Phys. **37**, 1383 (1998).
17) N. Shigekawa, N. Watanabe, and E. Higurashi, Proc. 3rd Int. IEEE Workshop Low-Temperature Bonding for 3D Integration, 2012, p. 109.
18) A. Pérez-Tomás, M. Lodzinski, O. J. Guy, M. R. Jennings, M. Placidi, J. Llobet, P. M. Gammon, M. C. Davis, J. A. Covington, S. E. Burrows, and P. A. Mawby, Appl. Phys. Lett. **94**, 103510 (2009).
19) M. M. R. Howlader, T. Watanabe, and T. Suga, J. Appl. Phys. **91**, 3062 (2002).
20) M. M. R. Howlader, H. Okada, T. H. Kim, T. Itoh, and T. Suga, J. Electrochem. Soc. **151**, G461 (2004).
21) H. Takagi, R. Maeda, N. Hosoda, and T. Suga, Jpn. J. Appl. Phys. **38**, 1589 (1999).
22) S. Nishida, J. B. Liang, M. Morimoto, N. Shigekawa, and M. Arai, Mater. Sci. Forum **778–780**, 718 (2014).
23) J. Liang, S. Nishida, M. Arai, and N. Shigekawa, Appl. Phys. Lett. **104**, 161604 (2014).
24) O. J. Guy, A. Pérez-Tomás, M. R. Jennings, M. Lodzinski, A. Castaing, P. A. Mawby, J. A. Covington, S. P. Wilks, R. Hammond, D. Connolly, S. Jones, J. Hopkins, T. Wilby, N. Rimmer, K. Baker, S. Conway, and S. Evans, Mater. Sci. Forum **615–617**, 443 (2009).
25) I. Konovalov, V. Strikha, and O. Breitenstein, Prog. Photovoltaics **6**, 151 (1998).
26) J. P. Donnelly and A. G. Milnes, IEEE Trans. Electron Devices **14**, 63 (1967).