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LETTER

Stability of diamond/Si bonding interface during device fabrication process

Jianbo Liang[1*], Satoshi Masuya[2], Seongwoo Kim[3], Toshiyuki Oishi[2], Makoto Kasu[2], and Naoteru Shigekawa[1]

[1]Department of Physical Electronics and Informatics, Graduate School of Engineering, Osaka City University, Sugimoto 3-3-138 Sumiyoshi-ku, Osaka 558-8585, Japan
[2]Department of Electrical and Electronic Engineering, Saga University, Honjo-machi 1, Saga 840-8502, Japan
[3]Adamant Namiki Precision Jewel Co., Ltd, Shinden 3-8-22 Adachi-ku, Tokyo 123-8511, Japan

*E-mail: liang@elec.eng.osaka-cu.ac.jp

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Diamond/Si bonding interface with an entire contact area and high thermal stability is achieved by surface activated bonding method. The fabrication of diamond field-effect transistors (FETs) on the diamond bonded to Si is demonstrated. The FET exhibits clear saturation and pinch-off characteristics. A 5 nm thick Si_xC_{x-1} layer was formed at the interface with annealing at 1000 °C. The layer was formed by the inter-diffusion of carbon and Si atoms near the bonding interface, which plays a role of residual stress relaxation between diamond and Si. These results suggest that diamond/Si heterostructures are applicable for combining diamond devices with Si LSI. © 2018 The Japan Society of Applied Physics

Diamond is an excellent semiconductor material with an ultra-wide band gap (5.47 eV) and possesses such as high carrier mobility (4500 $cm^2 V^{-1} \cdot s$ for electron and 3800 $cm^2 V^{-1} \cdot s$ for hole),[1)] high saturation velocity (1.5×10^7 cm s^{-1} for electron and 1.05×10^7 cm s^{-1} for hole), high chemical inertness, and the highest electrical breakdown field strength (>10 MV cm^{-1}) among semiconductor materials.[2)] Therefore, diamond is the best potential candidate as the next generation semiconductor material for high power and high frequency electronic devices. Furthermore, Johnson's figure of merit exhibits that RF power capability of diamond is 3 times higher than that of SiC.[3)] Additionally, diamond which possesses the highest thermal conductivity among materials, higher than GaN and SiC, is the most promising material as a superior heat spreading substrate for power devices.

Single-crystal diamond (SCD) with high quality is necessary for the practical application of diamond devices. However, large SCD is difficult to be obtained by the high pressure high temperature (HPHT) method, which limits the development of diamond device technology. SCD is currently limited to an area of 8×8 mm^2, which is much smaller than Si (450 mm in diameter). It is necessary to have a minimum size in 2 inches for fabricating diamond devices using current semiconductor production line. The combination of SCD and Si would be a very effective approach for fabricating diamond-based power devices using Si process facilities and the integration of diamond devices and Si LSI with various functions on the same substrate. It has been reported that the bonding of SCD and Si was performed using an Au intermediate layer for the heat dissipation of power device.[4)] However, the bonding interface with a metal layer is not suitable for high frequency application and is difficult to withstand the process of diamond device fabrication.

The direct bonding of dissimilar materials at room temperature has been achieved by surface activated bonding (SAB) technique. SAB was used for fabricating a variety of heterostructures such as GaAs/Si,[5)] 4H-SiC/Si,[6)] GaAs/SiC,[7)] and GaAs/GaN,[8)] heterostructures. The direct bonding of SCD and Si by SAB was demonstrated by J. Liang et al.[9)] In the previous paper, diamond/Si bonding interface with full contact area and high thermal stability were not achieved. Although the heating of the bonding samples is not required during SAB process, a high temperature of about 1000 °C lasting long time is necessary for the diamond epitaxial growth.[10,11)] A much large lattice mismatch between diamond ($a = 3.57$ Å) and Si ($a = 5.43$ Å) makes the thermal stability of diamond/Si bonding interface difficult. The thermal stability and reliability of the bonding interface are very important for fabricating diamond device and combining diamond device with Si LSI.

In this letter, we report the fabrication of diamond/Si bonding interface with an entire area of 4×4 mm^2 and demonstrate the fabrication of diamond field-effect transistors (FETs) on diamond bonded to Si. The electrical properties of the FETs were characterized by measuring their current–voltage (I–V) characteristics. The thermal stability of the bonding interface was tested at 1000 °C in N_2 gas ambient pressure. The bonding interface was investigated by transmission electron microscopy (TEM) observation and the C1s and Si 2p spectra of diamond/Si bonding interface without and with annealing at 1000 °C after removing Si by mechanical polishing and wet etching using KOH solution at 50 °C were characterized by X-ray photoelectron spectroscopy (XPS).

Figure 1 shows a schematic of the diamond FET fabrication process on diamond bonded to Si. A HPHT synthetic Ib type (100) SCD with a size of 4 mm × 4 mm × 0.55 mm was bonded to a n-Si (100) substrate with a size of 15 mm × 25 mm × 0.53 mm by means of SAB.[12)] Prior to the bonding, the diamond surface was polished by chemical-mechanical polishing. The averaged roughness (Ra) of diamond and Si surfaces were measured to be 0.32 nm and 0.25 nm, respectively, by an atomic force microscope. After bonding, a p-type diamond layer was deposited on the HPHT diamond by microwave plasma assisted chemical vapor deposition (MWCVD). Prior to the diamond layer deposition, the diamond/Si bonded sample was cleaned with acetone and ethanol in an ultrasonic bath for 300 s, dried under N_2. During deposition, the methane concentration, plasma power, substrate temperature, and chamber pressure were 1%, 750 W, ~930 °C, and 50 Torr, respectively. The growth rate was 0.5 $\mu m\, h^{-1}$ and the thickness of the deposited p-type layer was 1 μm. The impurity concentration was not introduced intentionally.

H-surface termination was performed by exposing diamond surface to H plasma in the MWCVD reactor. The H-terminated diamond surface was exposed to 2% NO_2 gas

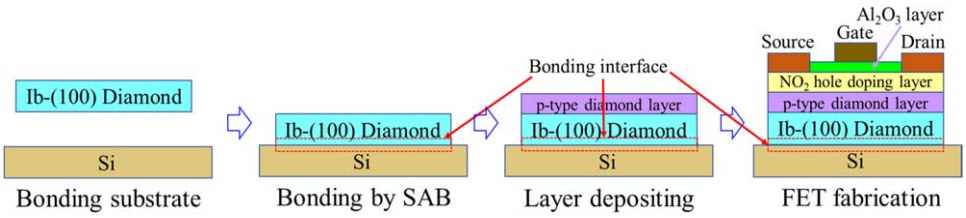

Fig. 1. (Color online) Schematic of the diamond FET fabrication process on diamond bonded to Si substrate.

diluted with N_2 gas (purity 5 N) for 10 min. The adsorbed NO_2 could increase hole concentration in the deposited diamond layer.[13,14] And then, Au ohmic contacts as source and drain electrodes were fabricated on H-terminated diamond surface using photolithography and lift-off techniques. To passivate the NO_2 adsorbed H-terminated diamond surface, an Al_2O_3 over-layer with a thickness of 16 nm was deposited by atomic layer deposition technique in the atomic layer-by-layer mode at 180 °C. Trimethylaluminum and H_2O were used as a source of Al and O, respectively. The deposition process of Al_2O_3 layer was the same as that reported for high performance diamond power FETs.[15] Finally, the gate electrode was formed by Al deposition on the deposited Al_2O_3 layer and the lift-off technique. An optical microscope image of the diamond FETs fabricated on diamond bonded to Si substrate is shown in Fig. 2.

The *I*–*V* characteristics of the FETs were measured using a semiconductor parameter analyzer (Agilent:4156 A). The diamond/Si bonded sample was annealed at 1000 °C for 5 min and 12 h in N_2 gas ambient pressure. The chemical bonding structures of the bonded interface without and with annealing at 1000 °C were evaluated by XPS (ESCA-3400) with a monochromatic Mg $K\alpha$ X-ray radiation source. The interfacial structures of diamond/Si heterostructure were investigated using TEM (JEM-2200FS).

The optical microscope images of the diamond/Si bonded sample surface without and with annealing at 1000 °C are shown in Figs. 3(a) and 3(b), respectively. No fringe patterns due to unbonded regions were observed on diamond/Si bond area, indicating that an entire area bonding of diamond and Si was achieved. Even for the diamond/Si bonded sample annealed at temperature as high as 1000 °C, the reduction in the bonded area was not observed, which is as same as that of the bonded sample without annealing. These results indicated that the bonding interface has a good thermal stability when a 1000 °C thermal load is applied. In addition, the bonding interface annealing at 1000 °C for 12 h was also conducted (not shown in the figure), no change in the bonded area was observed.

A low and high magnification cross-sectional TEM images of the diamond/Si bonding interface with annealing at 1000 °C are shown in Figs. 4(a) and 4(b), respectively. A straight line indicates the center of the bonded sample corresponding to the bonding interface between diamond and Si. A significant contrast was observed between diamond and Si in regions of 10 nm away from the bonding interface, which originates from the elastic deformation of diamond and Si by the residual strain. It is noted that most regions of the bonding interface are smooth, and no voids or fractures were observed at the interface, which suggests that the surface atoms of diamond

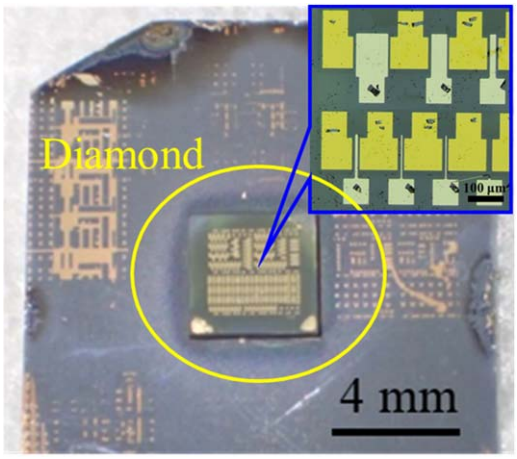

Fig. 2. (Color online) A optical microscope image of the diamond FETs fabricated on diamond bonded to Si substrate (the inset shows a top view image of diamond FETs).

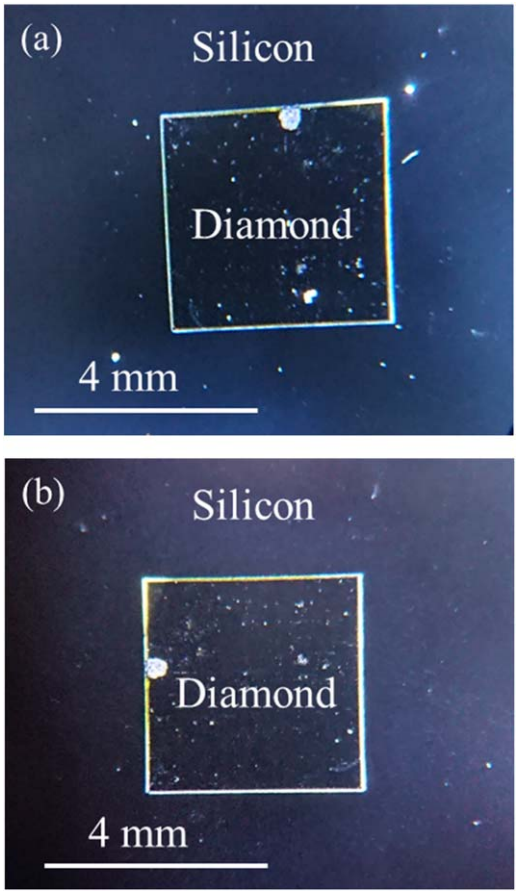

Fig. 3. (Color online) The optical microscope images of the diamond/Si bonded sample surface without (a) and with annealing at 1000 °C (b).

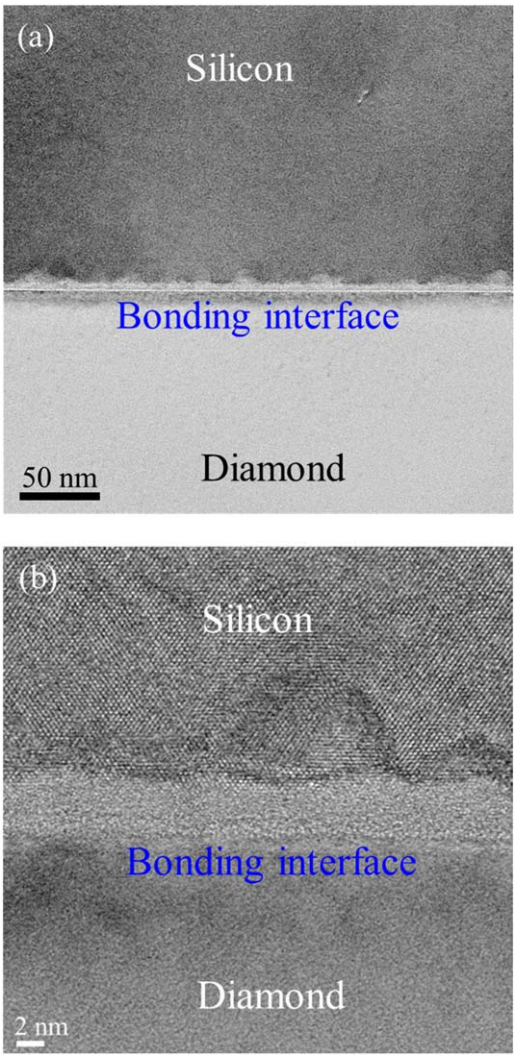

Fig. 4. (Color online) A low (a) and high magnification (b) cross-sectional TEM images of the diamond/Si bonding interface with annealing at 1000 °C.

and Si had directly bonded each other. As shown in Fig. 4(b), we found that an intermediate layer with a thickness of about 5 nm was formed at the bonding interface and a part of intermediate layer is irregularly structured close to the Si side of the bonding interface.

The C1s and Si 2p spectra of the diamond/Si bonding interface without and with annealing at 1000 °C are shown in Figs. 5(a) and 5(b), respectively. The spectra were fitted assuming a Gaussian function using Shirley's method after the backgrounds subtraction. As shown in Fig. 5(a), the C1s spectrum of the bonding interface without annealing was decomposed into component located at 285.4, 286.4, and 289.4 eV. These are assigned to sp^2 and sp^3 bonded carbons, and C–O/C–O–C bonding state, respectively.[16,17] For the diamond/Si bonding interface without annealing, no any components were detected in the Si 2p spectrum of the bonding interface [Fig. 5(a)].

For the diamond/Si bonding interface with annealing at 1000 °C [Fig. 5(b)], the C1s spectrum was decomposed into two peaks located at 282.7 and 283.6 eV. These are attributed to Si–C and C–H chemical bonding states, respectively. We should note that no sp^2 and sp^3 component peaks were observed in the C1s spectrum of diamond with annealing at 1000 °C. This indicates that amorphous carbon or graphite and diamond components were eliminated after annealing at 1000 °C. Figure 5(b) shows that the Si 2p spectrum was decomposed into two peaks located at the binding energy of 100.6 and 101.2 eV. These peaks are attributed to Si–C and C–O–Si bonds, respectively.

Figure 6 shows the drain current (I_{DS}) and drain bias (V_{DS}) characteristics of diamond FET with a gate length (L_G) of 3 μm and gate width (W_G) of 300 μm on diamond bonded to Si. The gate bias (V_{GS}) was varied from −4 to 10 V with a voltage step of 2 V. The FET shows normally-on characteristics, and the channel is pinched off at $V_{GS} = 10$ V. As the V_{GS} decrease, the saturation current increases. The maximum I_{DS} and transconductance (g_m) are obtained to be 43.5 mA mm^{-1} and 4.6 mS mm^{-1}, respectively. The maximum I_{DS} is smaller than those for diamond FETs,[18,19] which attributed to the long gate length and the short time of exposing NO_2 gas. The threshold voltage (V_{TH}) and the pinch-off voltage (V_P) of FET are estimated to be 8 V and 9.3 V, respectively, and the acceptor concentration (N_A) of the deposited diamond layer is calculated to be 5.8×10^{15}cm^{-3} from the $I_{DS}-V_{DS}$ characteristics.

The $sp^3/(sp^2 + sp^3)$ ratio calculated was estimated from the integrated intensity of the sp^2 and sp^3 peaks to be about 25.4%. The lower $sp^3/(sp^2 + sp^3)$ ratio may be due to a part of diamond on the surface was decomposed into amorphous carbon by Ar beam irradiation. It has been reported that the diamond film was changed to amorphous carbon by ion irradiation.[20] The observed C–O/C–O–C, C–H, and C–O–Si bonds should be resulted from hydrocarbon and oxide formed on the surface of diamond during Si removal processes. We found that Si–C bond was observed in the C1s and Si 2p spectra after annealing at 1000 °C. This indicates that diamond bonded to Si forms a thin Si_xC_{1-x} layer at the interface after annealing at 1000 °C. This result is consistent with the intermediate layer formed at the bonding interface with annealing at 1000 °C.

It has been reported that the thickness of the amorphous layer formed at the bonding interface strongly depended on the post-annealing temperature, which decreased with increasing annealing temperature and the amorphous layer finally disappeared after annealing at a certain temperature due to the recrystallization of the amorphous layer.[21,22] After annealing process, the thinned amorphous layer would be much more difficult to relax the residual stress caused by thermal expansion coefficient mismatch between diamond and Si. The observed Si_xC_{1-x} intermediate interface layer should be formed by the inter-diffusion of carbon and silicon atoms near the bonding interface at high annealing temperatures. Instead of the amorphous layer the intermediate interface layer played a role of relaxation layer, which enables the diamond/Si bonding interface to have a good thermal stability. On the other hand, we performed a simple bonding strength test, in which the separation of diamond and Si was not observed when a load of 300 N applied to the cross section of diamond. More importantly, no structural defects such as cracks were observed at the interface with annealing at as high as 1000 °C, and no diamond separation were observed during diamond FETs fabrication. These mean that

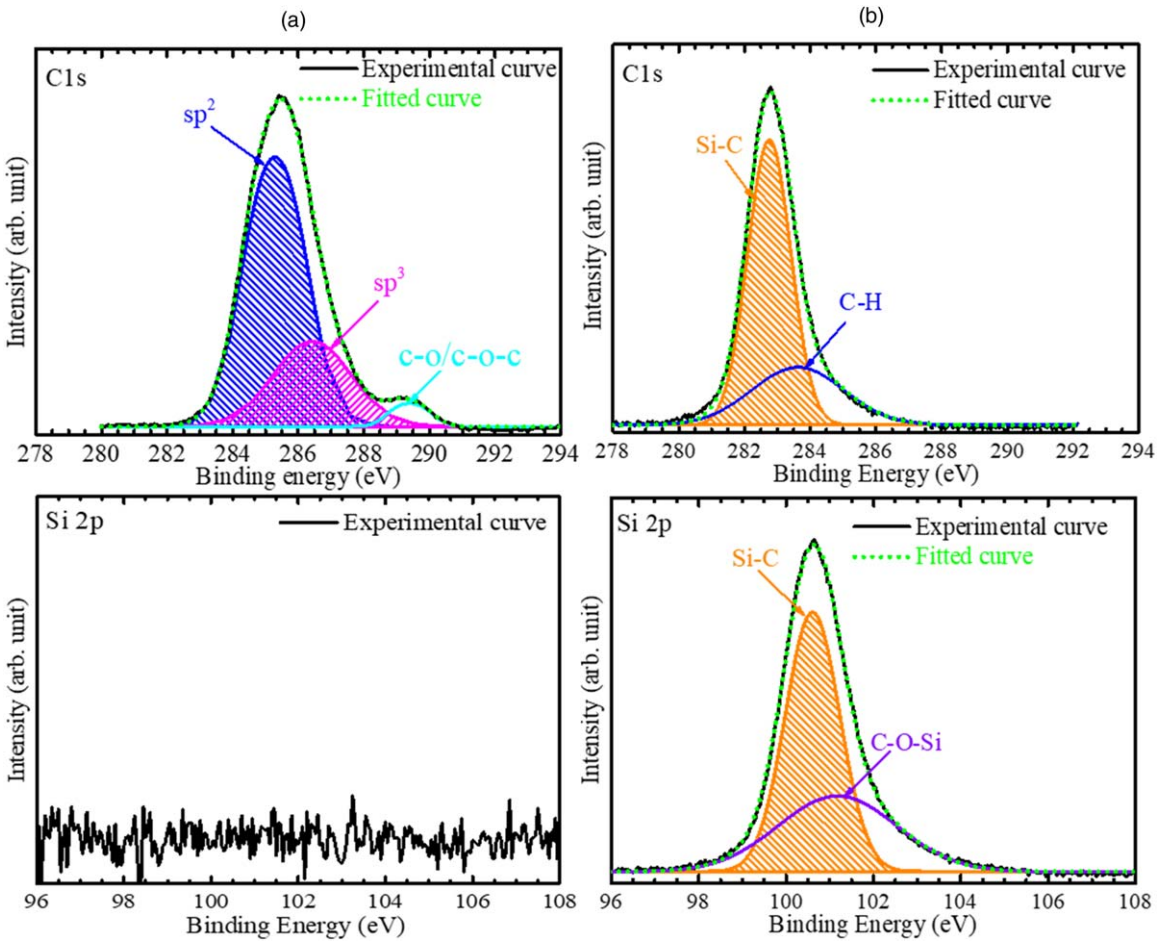

Fig. 5. (Color online) C1s and Si 2p spectra of diamond/Si bonded sample interface without (a) and with annealing at 1000 °C (b).

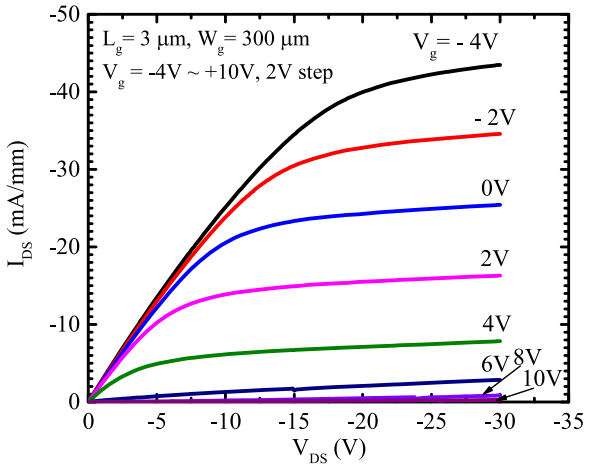

Fig. 6. (Color online) I_{DS}–V_{DS} characteristics for various gate voltages V_{GS} of p-channel diamond FETs with a NO_2 absorbed H-terminated diamond surface and an ALD Al_2O_3 over-layer.

the diamond/Si bonding interface could withstand the semiconductor device fabrication process and temperature less than 1000 °C.

In summary, diamond/Si bonding interface with a bonding area of $4 \times 4\,mm^2$ was achieved by SAB at room temperature. The thermal stability of the bonding diamond/Si interface and the fabrication of diamond FETs on diamond bonded to Si were demonstrated. No reduction in the bonding area and any mechanical cracks were observed at the bonding interface after annealing at temperature as high as 1000 °C. The FET exhibited normally-on behavior with clear pinched-off characteristics at room temperature. An intermediate layer with a thickness of 5 nm was observed at the bonding interface after annealing at 1000 °C, which was determined to be Si_xC_{1-x} layer by XPS measurements.

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