

Optimization of AlGa_N-based spacer layer for InAlN/GaN interfaces

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AlGa_N-based spacer layers for lattice-matched and nearly lattice matched InAlN/GaN interfaces were examined in Al₂O₃/InAlN/AlGa_N/AlN/GaN structures. An Al₂O₃ overlayer was deposited to investigate the characteristics under positive bias by capacitance-voltage (*C-V*) measurement. The *C-V* characteristic for a sample with an Al_{0.38}Ga_{0.62}N/AlN double spacer layer indicated unfavorable electron accumulation at the InAlN/AlGa_N interface inside the barrier under positive bias. To suppress the unfavorable accumulation, attempts were made to increase the Al molar fraction of the AlGa_N layer to reduce the

conduction band discontinuity and interface charge at InAlN/AlGa_N interface. An Al_{0.44}Ga_{0.56}N/AlN double spacer layer and an Al_{0.44}Ga_{0.56}N single spacer layer of almost the same total thickness were investigated. Although both spacer layers result in normal *C-V* characteristics without the indication of unfavorable electron accumulation, the InAlN layer on a 1.5-nm-thick Al_{0.44}Ga_{0.56}N single spacer layer exhibited superior surface morphology without deteriorating the mobility of the two-dimensional electron gas despite the absence of the AlN layer.

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1 Introduction An InAlN/GaN heterostructure provides a high-density two-dimensional electron gas (2DEG) owing to the difference in spontaneous polarization at the interface [1, 2]. To enhance electron mobility, an AlN ultrathin layer has been used as a conventional spacer layer [3, 4]. Several reports have been published on the application of the InAlN/AlN/GaN structure to field-effect transistors (FETs) [3–5]. A recent study [6], however, reported that the insertion of an Al_{0.38}Ga_{0.62}N/AlN double spacer layer improved surface flatness and electron mobility compared with those for a single AlN spacer layer. More recently, we have proposed the use of an Al_{0.44}Ga_{0.56}N alloy for a spacer layer at a lattice-matched InAlN/GaN interface [7].

In this paper, we report more detailed results on an investigation of the effectiveness of AlGa_N-based spacer layers for lattice-matched and nearly lattice matched InAlN/AlGa_N heterointerfaces. Samples with an Al_{0.38}Ga_{0.62}N/AlN double spacer layer, with an

Al_{0.44}Ga_{0.56}N/AlN double spacer layer, and with an Al_{0.44}Ga_{0.56}N single spacer layer were fabricated and tested. To investigate characteristics under positive bias by capacitance-voltage (*C-V*) measurement, an Al₂O₃ insulator overlayer was deposited. We discuss the advantages of an Al_{0.44}Ga_{0.56}N single spacer layer without an AlN layer over Al_{0.38}Ga_{0.62}N/AlN and Al_{0.44}Ga_{0.56}N/AlN double spacer layers revealed in this study.

2 Experimental Figure 1 shows the structures of the tested samples with three different types of AlGa_N/AlN spacer layers, *i.e.*, Al_{0.38}Ga_{0.62}N (6 nm)/AlN (0.75 nm) (type A), Al_{0.44}Ga_{0.56}N (1 nm)/AlN (0.44 nm) (type B), and Al_{0.44}Ga_{0.56}N (1.5 nm) (type C). The fabrication process of the samples was as follows. Heterostructures were grown by metal organic vapor phase epitaxy (MOVPE). Details of the growth conditions have been reported previously in Ref. [6]. For the cap-annealing process used to form an ohmic contact, a 20-nm-thick SiN_x layer was deposited by elec-

tron-cyclotron resonance chemical vapor deposition (ECR-CVD) using a SiH_4/Ar and N_2 gas mixture at 260 °C. After opening a ring-shaped window by lithography and wet etching using buffered hydrofluoric acid (BHF, HF: NH_4F = 1 : 5) solution, a ring-shaped Ti/Al/Ti/Au (30 nm/50 nm/20 nm/100 nm) ohmic electrode was formed. Then the samples were annealed in N_2 ambient at 800 °C for 1 min. After removing the SiN_x layer using BHF solution, an Al_2O_3 overlayer was deposited by atomic layer deposition (ALD) at a substrate temperature of 250 °C by alternate pulse injections of H_2O vapor and trimethylaluminum. Finally, a circular Ni/Au (20 nm/ 50 nm) electrode was formed in the center of the ohmic ring.

sample 1 was low, limiting the maximum applied voltage, presumably because the thickness was too small to achieve a high resistivity owing to the unoptimized surface pre-treatment before ALD. The C-V curve of sample 1 exhibited anomalous saturation at approximately 130 pF under low positive bias in spite of the much higher insulator capacitance, C_1 , value shown in Table 1. This saturation indicated that electron accumulation occurred at the InAlN/AlGaN interface. This phenomenon may become a drawback of this heterostructure if it is applied to an FET gate, resulting in parallel conduction and a complicated change in potential.

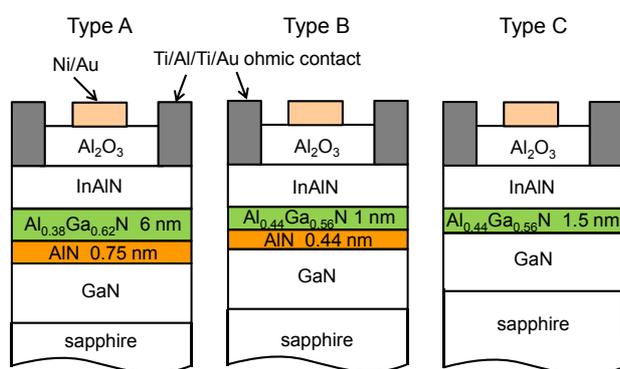


Figure 1 Schematic sample structures.

3 Results and discussion Table 1 summarizes the results of Hall measurements for 2DEGs before Al_2O_3 deposition and details of the completed sample structure for all samples. The thickness of each layer was controlled by the growth rate so that the intended thickness values have been described for samples 1 and 3 in our previous report [7]. Here these values were reappraised by considering the C-V characteristics. In Table 1, μ and n_s indicate measured electron mobility and sheet carrier density, respectively. Sufficiently high values of μ and n_s were obtained for all the samples. Sample 1 with an $\text{Al}_{0.38}\text{Ga}_{0.62}\text{N}/\text{AlN}$ double spacer layer exhibited the highest electron mobility, indicating the most effective suppression of alloy scattering among the samples. However, important information was obtained by C-V measurement after Al_2O_3 overlayer deposition as discussed below.

The C-V curve for sample 1 is plotted in Fig. 2 by the broken line. The breakdown voltage of the Al_2O_3 layer of

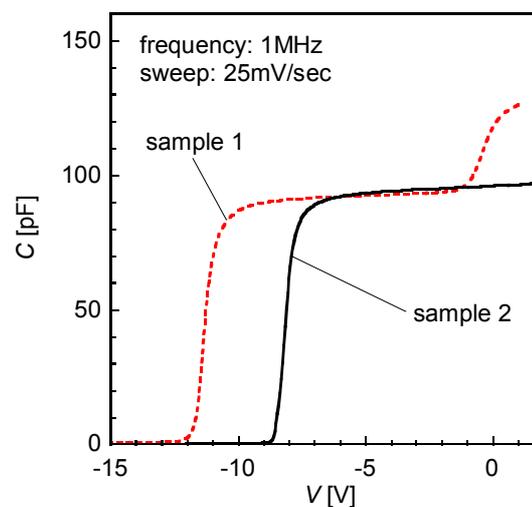


Figure 2 C-V characteristics for samples 1 (broken line) and 2 (solid line) with an $\text{Al}_{0.38}\text{Ga}_{0.62}\text{N}/\text{AlN}$ spacer layer and an $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}/\text{AlN}$ spacer layer, respectively.

According to previous reports, the $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{Al}_{0.38}\text{Ga}_{0.62}\text{N}$ interface is characterized with a lower conduction band edge, E_C , location of AlGaN [8-10] than that of InAlN and the positive interface charge owing to the difference in spontaneous polarization between two alloys [1]. The unfavorable electron accumulation is considered to have resulted from these characteristics being enhanced by the relatively large thickness of the AlGaN layer as schematically shown in Fig. 3. A means of excluding unfavorable electron accumulation is therefore to use a thinner AlGaN layer that achieves a reduction in the conduction band discontinuity, ΔE_C , and the interface charge at the interface with InAlN.

Table 1 Detail of fabricated samples.

sample number	structure type	$\text{In}_x\text{Al}_{1-x}\text{N}$ layer		Hall measurement results		Al_2O_3 overlayer	
		x	thickness [nm]	n_s [cm^{-2}]	μ [$\text{cm}^2/\text{V}\cdot\text{s}$]	thickness [nm]	C_1 [pF]
1	A	0.17	10	2.2×10^{13}	1400	10	260
2	B	0.19	12	1.9×10^{13}	1100	13	200
3	C	0.18	12	2.1×10^{13}	1100	14	190
4	C	0.20	12	1.8×10^{13}	1200	11	230

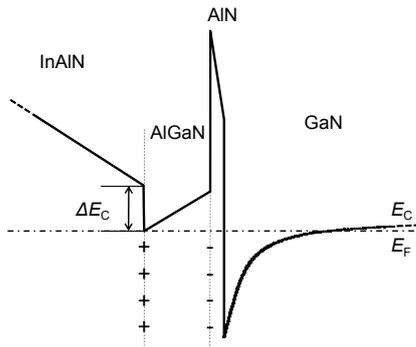


Figure 3 Schematic E_C diagram near the barrier/GaN interface of the InAlN/AlGa_xN/AlN/GaN heterostructure for the AlGa_xN layer with a molar fraction leading to unfavorable electron accumulation at the InAlN/AlGa_xN interface.

As a guide for material design, E_C and interface charge density, σ , calculated according to the theoretical estimation [1, 8] and experimental results [9, 10] are plotted as functions of molar fraction x in Fig. 4 for InAlN and AlGa_xN alloys and their interfaces. It can be seen that an increase in the Al molar fraction of the AlGa_xN layer results in decreases in ΔE_C and σ at the InAlN/AlGa_xN interfaces. However, an excessively large increase in the Al molar fraction might result in the failure of epitaxial growth owing to the large mismatch. Actually, it has been reported that the surface morphology was deteriorated by the growth of 1 nm of AlN on GaN [6]. We therefore decided to increase the Al molar fraction of the AlGa_xN layer slightly from 0.38 to 0.44. In Fig. 4, fine dotted lines are plotted to assist the comparison of σ between InAlN/Al_{0.38}Ga_{0.62}N and InAlN/Al_{0.44}Ga_{0.56}N interfaces. It can be seen that a smaller values of σ were predicted at the InAlN/Al_{0.44}Ga_{0.56}N interfaces.

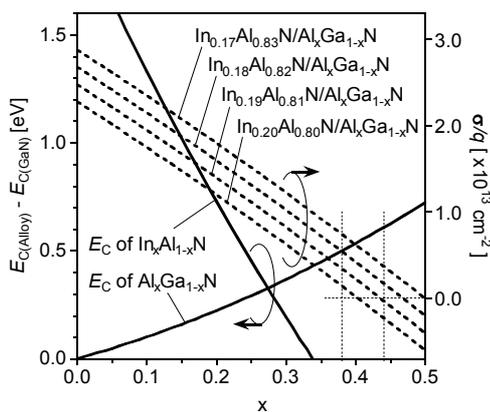


Figure 4 Plot of theoretical estimations. Solid lines indicate E_C for In_xAl_{1-x}N and Al_xGa_{1-x}N relative to that for GaN. Broken lines indicate σ divided by the elemental charge, q , at the interface between InAlN (with fixed x) and Al_xGa_{1-x}N. Both are plotted as functions of x assuming pseudomorphic conditions.

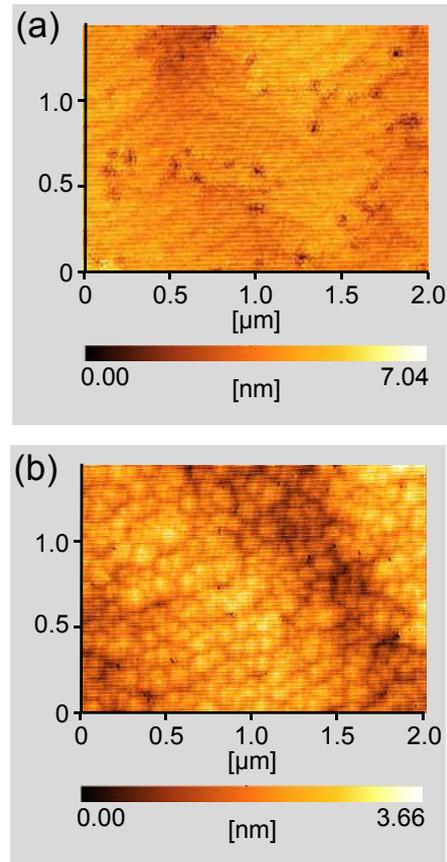


Figure 5 AFM images obtained for the surface of (a) In_{0.19}Al_{0.81}N (12 nm)/Al_{0.44}Ga_{0.56}N (1 nm)/AlN (0.44 nm)/GaN and (b) In_{0.18}Al_{0.82}N (12 nm)/Al_{0.44}Ga_{0.56}N (1.5 nm)/GaN structures.

First, we examined the Al_{0.44}Ga_{0.56}N/AlN double spacer layer. We fabricated sample 2 that had a type B structure with reduced AlGa_xN thickness of 1 nm. As expected, the C - V characteristics for sample 2 with an Al₂O₃ overlayer did not exhibit the anomalous capacitance step due to electron accumulation at the InAlN/AlGa_xN interface as shown in Fig. 2, by the solid line. However, an atomic force microscope (AFM) image of the surface of sample 2, taken at the fabrication step after epitaxial growth before Al₂O₃ deposition, indicated large pits as shown in Fig. 5(a). Even though the electron mobility was sufficiently large for device application, it was likely that the insertion of the AlN layer beneath the Al_{0.44}Ga_{0.56}N layer made the growth condition severe.

If the Al_{0.44}Ga_{0.56}N single layer can fill the role of a spacer layer without causing any unfavorable phenomena, it will be beneficial for device fabrication by simplifying the growth process. We next attempted to fabricate samples with the Al_{0.44}Ga_{0.56}N single layer. To determine the optimum thickness of the Al_{0.44}Ga_{0.56}N layer, we investi-

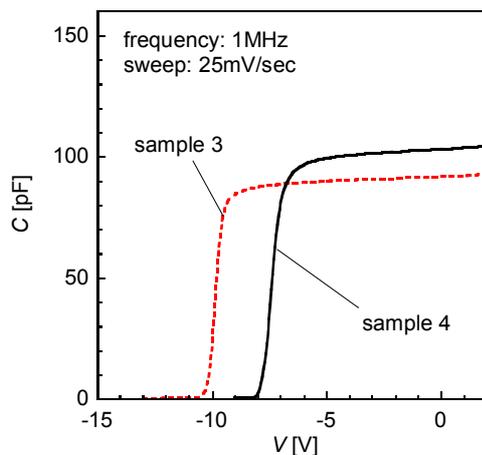


Figure 6 C - V characteristics for samples 3 and 4 with $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ single spacer layers.

gated the thickness dependence of the surface morphology of $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ layers on GaN by using AFM. When the thickness of the $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ layer was greater than 1.5 nm, AFM images showed the number and size of pits increased remarkably. Thus we attempted to grow InAlN layers on the $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ (1.5 nm)/GaN structure, which resulted in a superior surface morphology as shown in Fig. 5(b). The surface morphology of the 1.5-nm-thick AlGaIn layer was greatly improved compared with that of 1.0-nm-thick AlN on GaN reported in Ref. [6], which led to a smoother InAlN/AlGaIn/GaN surface (root mean square roughness (rms): 0.35 nm) than that of the conventional InAlN/AlN/GaN (rms: 0.53 nm) structure [6].

To investigate the electrical characteristics of the 1.5-nm-thick $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ single spacer layer, the type C sample was fabricated. As shown in Table 1, samples 3 and 4 consisted of InAlN with $x = 0.18$ and 0.20 , respectively. The electron mobilities of the 2DEGs for samples 3 and 4 before Al_2O_3 deposition did not deteriorate despite the absence of the AlN layer. The C - V characteristics of samples 3 and 4 after fabrication are shown in Fig. 6. The anomalous saturation resulting from electron accumulation at the InAlN/AlGaIn interface was not observed in both samples. In addition, the location of the capacitance step corresponding to 2DEG depletion shifted depending on the Al-molar fraction of the InAlN layer. The amount of the observed shift was in good agreement with the values calculated theoretically, which indicated that excellent hetero-interfaces were formed in both samples.

4 Summary AlGaIn-based spacer layers for InAlN/GaN interfaces were examined in $\text{Al}_2\text{O}_3/\text{InAlN}/\text{AlGaIn}/\text{AlN}/\text{GaN}$ structures. The C - V characteristic for the sample with an $\text{Al}_{0.38}\text{Ga}_{0.62}\text{N}$ (6 nm)/AlN (0.75 nm) double spacer layer exhibited unfavorable electron accumulation at the InAlN/AlGaIn interface inside the barrier. To solve this problem, an attempt was made to increase the Al molar fraction of the AlGaIn layer to reduce ΔE_C and σ . Both an $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ (1 nm)/AlN (0.44 nm) double spacer layer and an $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ (1.5 nm) single spacer layer prevented unfavorable electron accumulation at $\text{In}_{0.18}\text{Al}_{0.82}\text{N}/\text{GaN}$, $\text{In}_{0.19}\text{Al}_{0.81}\text{N}/\text{GaN}$ and $\text{In}_{0.20}\text{Al}_{0.80}\text{N}/\text{GaN}$ interfaces. The $\text{Al}_{0.44}\text{Ga}_{0.56}\text{N}$ single spacer layer can achieve a superior surface morphology of the InAlN layer grown on it without deteriorating the 2DEG electron mobility despite the absence of an AlN layer in a simple heterostructure.

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