BRIEF NOTES

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BRIEF NOTE

Intrinsic microstructure of Si/GaAs heterointerfaces fabricated by surface-activated bonding at room temperature

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The intrinsic microstructure of Si/GaAs heterointerfaces fabricated by surface-activated bonding at room temperature is examined by plane-view transmission electron microscopy (TEM) and cross-sectional scanning TEM using damage-free TEM specimens prepared only by mechanochemical etching. The bonded heterointerfaces include an As-deficient crystalline GaAs layer with a thickness of less than 1 nm and an amorphous Si layer with a thickness of approximately 3 nm, introduced by the irradiation of an Ar atom beam for surface activation before bonding. It is speculated that the interface resistance mainly originates from the As-deficient defects in the former layer.

Tandem solar cells consisting of silicon (Si) and III–V compounds are one of the promising candidates for next-generation terrestrial photovoltaic systems that can surpass the efficiency milestone of 30% for non-concentrating solar cells without using expensive Ge or GaAs substrates.[1–3] However, Si/III–V heterointerfaces fabricated by epitaxial growth can introduce structural defects such as dislocations and cracks,[4,5] by which current flow is disturbed, because of mismatches in lattice constant and thermal expansion coefficient. Also, direct wafer bonding without adhesive or solder, such as hydrophilic, hydrophobic, and plasma-assisted bonding, can be applied to fabricate the hetero-interfaces.[6–9] The method requires, however, high-temperature annealing to obtain sufficient bonding strength[10] that can induce the intermixing of dopants and mechanical defects across the heterointerfaces. Alternatively, surface-activated bonding (SAB) at room temperature,[11] in which surfaces of substrates are activated before bonding by creating dangling bonds via the removal of contaminants under an energetic particle bombardment in high vacuum, is applied to form tough Si/III–V heterointerfaces without macro defects.[12] InGaP/GaAs//Si hybrid multijunction cells with a high efficiency up to 26% are demonstrated using the SAB method,[13,14] even though the estimated efficiency is still lower than the theoretical one of about 40%.[15]

In the SAB method, it is believed that an amorphous-like intermediate layer, less than 7–8 nm in thickness, is formed on the surfaces in the surface activation process.[16] In addition, the surface roughness after the activation process, depending on inert gas species and activation time,[17,18] degrades the bonding quality owing to microscopic gaps at the bonded interface.[19] It is pointed out that the intermediate layers on either side of the incompletely-bonded interface affect the electrical property.[20] Actually, the resistance of SAB-fabricated Si/GaAs interfaces, which is estimated to be on the order of $10^{-1}\,\Omega\,\mathrm{cm}^2$,[21,22] is markedly higher than that of defect-free IV/III–V interfaces fabricated by epitaxial growth (on the order of $10^{-4}\,\Omega\,\mathrm{cm}^2$).[23] The resistance of SAB-fabricated interfaces is decreased by annealing at low temperatures,[20,22,24,25] presumably owing to the annihilation of defects in the intermediate layers. Accordingly, a comprehensive knowledge of the electrical property at Si/III–V heterointerfaces depending on their atomistic structure is indispensable in the fabrication of tandem cells with higher efficiency by optimizing the interface structure.

The structural property of SAB-fabricated Si/GaAs heterointerfaces has been examined by cross-sectional transmission electron microscopy (TEM), in which the cross section of the interfaces is observed, using TEM specimens prepared by ion milling. Even though the structural modification due to ion milling is not taken into consideration, those data suggest that an amorphous-like layer of 3–5 nm thickness is formed at the interfaces,[12,13,22] and the layer is mainly composed of Si.[12,22] The latter hypothesis is supported by the fact that the thickness of the intermediate layer in SAB-fabricated Si/Si interfaces (6–9 nm)[16,17,24,26] is much larger than that in SAB-fabricated GaAs/GaAs interfaces (about 1–2 nm).[18] TEM also shows strain fields at the interfaces fabricated by the SAB of rough surfaces,[19] although their origin is unclear from the viewpoint of defect structure.

Here, we discuss the intrinsic microstructure of the intermediate layers in SAB-fabricated Si/GaAs heterointerfaces, by using damage-free TEM specimens prepared only by mechanochemical etching, without ion milling. TEM with the incident direction normal to the interfaces (so-called plane-view TEM), as well as cross-sectional TEM, reveals the structure and two-dimensional distribution of the intrinsic defects along the interfaces, which would degrade the interface resistance. This finding can provide guidance to optimize the microstructure of SAB-fabricated Si/III–V heterointerfaces for realizing high-efficiency hybrid tandem cells at a low cost.

Heterointerfaces of p-Si/n-GaAs were fabricated under a SAB condition.[14,21] We used a B-doped (001) p-Si substrate (with a carrier concentration of $2 \times 10^{14}\,\mathrm{cm}^{-3}$) cut from a commercial polished wafer grown by the Czochralski method. We also used a Si-doped n-GaAs substrate (with a carrier concentration of $2 \times 10^{16}\,\mathrm{cm}^{-3}$) with an n-GaAs/$n^+$-GaAs bilayer grown epitaxially on an n-GaAs substrate 5° off from (001) toward [110]. The surfaces of these substrates were cleaned with acetone and ethanol, and then activated by irradiating an Ar fast atom beam (with a current of 1.8 mA at an applied voltage of approximately 2.0 kV) for 180 s, in a high vacuum below 5×10^{-5} Pa. Immediately after the activation process, the substrates were brought into contact

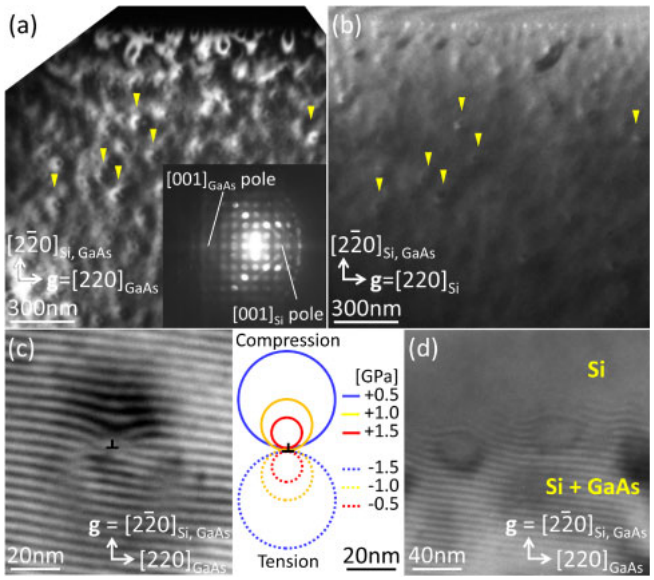

Fig. 1. (Color online) Plane-view dark-field images of crystalline (a) GaAs and (b) Si at a Si/GaAs heterointerface taken with the (220) reflections for GaAs and Si, respectively. The inset in (a) shows the TED pattern obtained with the incident direction nearly normal to the interface. (c and d) Plane-view bright-field images of the interface taken with both the (2$\bar{2}$0) reflections for Si and GaAs due to (c) a dislocation in GaAs cropping out the interface and (d) dimples on the GaAs surface. The inset in (c) indicates the calculated hydrostatic stress field for dislocations in GaAs.

and pressed for 60 s at 10 MPa at room temperature. Also, p-Si/p-Si and n-GaAs/n-GaAs homointerfaces were fabricated under the same SAB condition.

For the plane-view TEM of Si/GaAs heterointerfaces, the GaAs side was dimpled by mechanochemical etching with silica nanoparticles until Si cropped out, and the Si side was then polished mechanochemically until the bottom of the dimple was sufficiently thin for TEM. Similarly, damage-free thin foils with the cross sections of Si/Si and GaAs/GaAs homointerfaces were prepared only by mechanochemical etching.[27] We could not prepare damage-free specimens with the cross section of Si/GaAs heterointerfaces, since the etching rate for Si was more than 10 times higher than that for GaAs. Plane-view TEM was performed with a conventional microscope (JEOL JEM-2000EX), and cross-sectional scanning TEM (STEM) using a high-angle annular dark-field (HAADF) technique was performed with an analytical microscope (JEOL JEM-ARM200F) operated at 200 kV.

In transmission electron diffraction (TED) patterns for Si/GaAs heterointerfaces observed nearly normal to the interfaces, the (2$\bar{2}$0) Kikuchi band for Si overlapped with that for GaAs, while the Si(220) band was 5° away from the GaAs one [the inset in Fig. 1(a)]. Thus, we can observe selectively the crystalline GaAs and Si by choosing the (220) reflection for GaAs and Si, respectively [Figs. 1(a) and 1(b)]. No macro defect expanding along the interfaces, such as cracks and misfit dislocations, was observed in the investigated area of about $5 \times 5\,\mu m^2$, resulting in a low resistance at the interfaces.[21,22]

At the GaAs surface in a bonded heterointerface, which would be the boundary between the crystalline GaAs and the noncrystalline intermediate layer, hemispherical strain fields existed [Fig. 1(a)]. The fields distributed at the entire boundary, with the separations of about several ten nanometers. Similar strain fields were observed in SAB-fabricated interfaces by cross-sectional TEM, and they were attributed to surface undulations introduced after the surface activation process.[19] On the other hand, the contrast due to strain fields was rather weak at the Si surface in the same heterointerface, in comparison with that at the GaAs surface observed under the same reflection condition [Fig. 1(b)]. Weak hemispherical strain fields were observed at locations where large strains existed at the GaAs surface [indicated with the arrows in Figs. 1(a) and 1(b)]. These results indicate that the boundary between the crystalline Si and the noncrystalline intermediate layer was rather smooth, although undulations on the GaAs surface would induce small strains around the boundary.

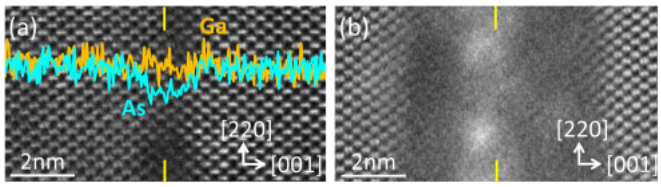

Fig. 2. (Color online) Cross-sectional HAADF-STEM images of (a) GaAs/GaAs and (b) Si/Si homointerfaces. The location of the bonded interface is indicated by the solid lines in each figure. The inset in (a) indicates the intensity profiles of X-rays for Ga and As across the interface.

By using both the (2$\bar{2}$0) reflections for Si and GaAs, moire fringes were observed, owing to the difference in lattice constant. In moire patterns obtained from a heavily strained location mentioned above, a circular area with a low number density of moire fringes coexisted with that with a high one, and they bordered each other along [2$\bar{2}$0] [Fig. 1(c)]. Therefore, a pair of compressive and tensile strain fields existed facing each other. This is the typical feature of edge dislocations,[28] and the pairs of circular areas would be explained with the calculated stress distribution for the edge dislocations expanding along [001] in GaAs with the Burgers vector of $a/2[110]$ [the inset in Fig. 1(c)]. This suggests that dislocations in GaAs cropping out Si/GaAs heterointerfaces would induce large strains at the interfaces.

When the thickness of the crystalline GaAs at the heterointerfaces was less than 2–3 nm, round contrasts without moire fringes, about a few ten nanometers in diameter, were observed in moire patterns [Fig. 1(d)]. This indicates that dimples would exist on the crystalline GaAs surface in the interfaces. Considering the size and distribution of the dimples, they would be the origin of the strain fields observed on the entire GaAs surface as in Fig. 1(a).

The microstructure of the intermediate layer was examined by cross-sectional HAADF-STEM of damage-free bonded homointerfaces. Unlike the previous report,[18] there was no amorphous-like layer at the GaAs/GaAs homointerfaces and the GaAs lattice arranged coherently across the interfaces [Fig. 2(a)]. The intermediate layer involved defects about 1–2 nm in size [the darker regions in Fig. 2(a)], in which As atoms were depleted by about 20% by Ar atom beam irradiation [the inset in Fig. 2(a)]. An amorphous layer of 5–8 nm thickness was introduced at the Si/Si homointerfaces [Fig. 2(b)], as reported.[16,17,24,26] Since the interfaces were fabricated at room temperature, compositional modification in the bonding process could be ignored. These results suggest that the intermediate layer in the bonded Si/GaAs

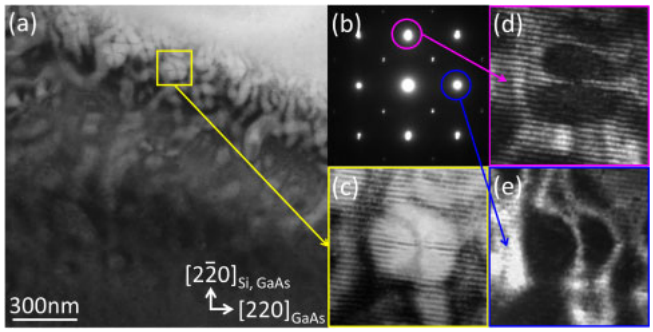

Fig. 3. (Color online) (a) Plane-view bright-field image of a Si/GaAs heterointerface irradiated with Ar ions, taken with the [001] incident for GaAs as in (b). (c) Enlarged image of the square area in (a). Dark-field images of the defect in (c), taken with the (d) $(2\bar{2}0)$ and (e) (220) reflections in (b).

interfaces would be composed of a defective crystalline GaAs layer with a thickness of less than 1 nm and an amorphous Si layer with a thickness of 3 nm.

We briefly discuss the origin of the resistance at the SAB-fabricated Si/GaAs interfaces. The resistance for the interfaces ($\sim 10^{-1}\,\Omega\,cm^2$),[22] as well as for GaAs/GaAs ones ($\sim 10^{1}\,\Omega\,cm^2$),[19] is higher than that for the Si/Si interfaces fabricated under a similar SAB condition ($\sim 10^{-3}\,\Omega\,cm^2$).[20] This suggests that the interface resistance would be mainly originate from the defects at the intermediate layer on the GaAs substrate. Actually, as a preliminary result, we found that strains due to the defects were reduced by annealing at 673 K,[29] by which the interface resistance is reduced.[22] Therefore, the resistance may be reduced by suppressing the As depletion in the surface activation process, via the optimization of SAB conditions. The introduction and annihilation processes of the As-deficient defects will be discussed in detail elsewhere.

Finally, we discuss the effect of ion irradiation on the structural property of TEM specimens. Figure 3(a) shows a bonded Si/GaAs interface in a TEM specimen finished with 3 keV Ar ion beam irradiation (with a current of about 25 mA) for 30 min. Unlike the specimens fabricated mechanochemically, round planar defects about 100 nm in diameter were introduced at the interfaces (Fig. 3). The platelets exhibited the characteristic bend contour contrast; they had a fourfold symmetry when both the (220) and $(2\bar{2}0)$ reflections were excited [Fig. 3(c)], while they had a twofold symmetry under two-beam reflection conditions [Figs. 3(d) and 3(e)]. A similar contrast was observed at microcracks in III–V compounds,[30] suggesting that the bonded interfaces were deteriorated by ion irradiation. The proposed amorphous-like intermediate layer on the GaAs surface in bonded interfaces of Si/GaAs[12,13,22] and GaAs/GaAs,[18] examined with TEM specimens prepared by ion milling, should involve the extrinsic defects. Therefore, damage-free specimens should be used to determine the intrinsic microstructure in SAB-fabricated interfaces.

In conclusion, the intrinsic microstructure of Si/GaAs heterointerfaces fabricated by SAB at room temperature was examined by plane-view TEM and cross-sectional STEM using damage-free TEM specimens prepared only by mechanochemical etching. The heterointerfaces would be composed of an As-deficient crystalline GaAs layer and an amorphous Si layer.

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