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Electrical conduction of Si/indium tin oxide/Si junctions fabricated by surface activated bonding

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The electrical properties of n^+-Si//indium tin oxide (ITO)/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions fabricated by surface activated bonding (SAB) were investigated. The current–voltage (*I–V*) characteristics of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions showed excellent linear properties. The interface resistances of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions were found to be 0.030, 0.025, and 0.029 Ω·cm^2, respectively, which are lower than required for concentrator photovoltaics. The interface resistances of all the junctions increased with increasing annealing temperature. The degradation of the interface resistance is lower in n^+-Si//ITO/n^+-Si junctions than in n^+-Si//ITO/p^+-Si and p^+-Si//ITO/n^+-Si junctions, when the annealing temperature is higher than 100 °C. These results demonstrate that the ITO thin film as an intermediate layer has high potential application for the connection of subcells in the fabrication of tandem solar cells.

1. Introduction

The III–V/Si-based tandem solar cell is one of the promising candidates for next-generation solar cells, which can provide high efficiency, low cost, and lightweight cells relative to conventional Si and III–V multijunction solar cells.[1–3] However, III–V/Si-based tandem cells formed by epitaxial growth typically introduce large cracks at the interface because of the mismatch in crystal lattice and thermal expansion coefficient.[4,5] Alternatively, a surface activated bonding (SAB) method has been applied to fabricate macroscopic defect-free III–V/Si heterointerfaces.[6,7] A variety of tandem cells such as InGaP/Si,[8] GaN/Si,[9] and GaInP/GaAs/Si[10,11] tandem solar cells were achieved by the SAB method, in which SAB-fabricated pn heterojunctions are used to connect the subcells.

The interface resistance would lead to large losses in the operation of multijunction solar cells,[12] owing to a large current density under concentrated sunlight illumination. The reduction in the electrical resistance across the bonding interface is very essential for realizing high-efficiency hybrid tandem cells. The electrical conductivity of the bonding interface could be improved by increasing the doping concentration of the bonding semiconductor.[12] In addition, it was reported that the interface resistance of SAB-fabricated junctions was decreased by annealing at low temperatures owing to the elimination of defects formed at the bonding interface.[13–16] However, the interface resistance ($\sim 10^{-1}$ Ω·cm^2) of SAB-fabricated GaAs/Si junctions[14] is still much larger than that of lattice-matched III–V/IV interfaces formed by epitaxial growth ($\sim 10^{-4}$ Ω·cm^2).[17] Therefore, it is necessary to further reduce the resistance of the bonding interface.

Indium tin oxide (ITO) has been widely applied in optoelectronic devices such as solar cells, light-emitting diodes, laser diodes, and photodetectors because it possesses a relatively low electrical resistivity on the order of 2×10^{-4} Ω·cm and a high transmittance in the visible range of the solar spectrum.[18–20] The ITO-layer-mediated junction is considered to be one of the most effective tools for enhancing the interface electrical conductivity. We previously successfully bonded an ITO thin film grown on Si substrates to Si substrates by the SAB method and found that the current–voltage (*I–V*) characteristics of the bonded samples revealed ohmic properties.[21] Although the heating of samples is not required during the SAB method, the effects of the annealing process on the electrical behavior of the bonded Si/ITO interfaces are necessary for obtaining low interface resistance.

In this work, we investigated the effects of the annealing process on the electrical properties of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions fabricated by SAB by measuring *I–V* characteristics and explored the transport properties of carriers across the bonding interfaces. The structural properties of the bonded interfaces were examined by field emission scanning electron microscopy (FE-SEM).

2. Experimental methods

ITO films of 90 nm thickness were grown on both p^+-Si and n^+-Si substrates by the reactive plasma deposition method.[22] The Hall measurements at room temperature revealed that the resistivities and carrier concentrations of p^+-Si and n^+-Si substrates are 0.003 Ω·cm and 2.64×10^{19} cm^{-3}, and 0.002 Ω·cm and 2.64×10^{19} cm^{-3}, respectively. ITO films grown on p^+-Si and n^+-Si substrates were bonded to p^+-Si and n^+-Si substrates, respectively, by SAB at room temperature,[23–26] so that n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions were fabricated. After bonding, Al/Ni/Au and Ti/Au multilayers were deposited on the back surfaces of the p^+-Si and n^+-Si substrates of the bonded samples, respectively. Ohmic contacts of ITO/p^+-Si and ITO/n^+-Si junctions were formed by evaporating Al/Ni/Au multilayers on the backside of p^+-Si substrates and Ti/Au multilayers on the backside of n-Si substrates and the surfaces of ITO films, respectively. ITO/p^+-Si, ITO/n^+-Si, n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions were annealed at different temperatures (100, 200, 300, and 400 °C) for 300 s in N_2 gas ambient. All the samples were diced into 2×2 mm^2 pieces. We measured their *I–V* characteristics using an Agilent B2902A at room temperature and investigated the bonded interfaces using FE-SEM (JEOL JSM6500F).

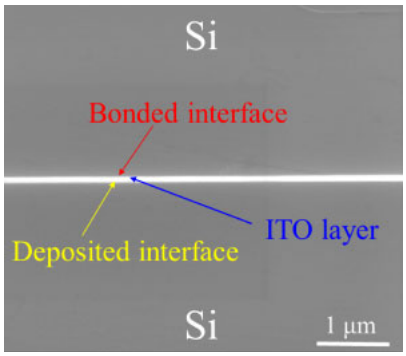

Fig. 1. (Color online) Cross-sectional FE-SEM image of the Si//ITO/Si interface.

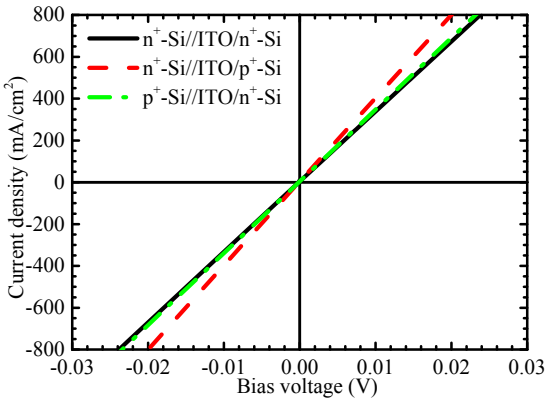

Fig. 2. (Color online) *I–V* characteristics of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions measured at room temperature.

3. Results

The cross-sectional FE-SEM image of the bonded Si//ITO/Si interface is shown in Fig. 1. An intermediate layer of about 90 nm thickness was observed at the center of the bonded interface, which corresponds to the ITO layer. Two straight lines between the top Si and the bottom Si can be clearly recognized at both sides of the ITO layer, which correspond to the bonded interface and the plasma-sputtering-deposited interface. There were no structural deficits or hollow spaces observed along the bonded interface. Figure 2 shows the *I–V* characteristics of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions measured between −0.03 and 0.03 V at room temperature. We found that the *I–V* characteristics shown in this figure revealed excellent linear properties. The interface resistances of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions were estimated to be 0.030, 0.025, and 0.029 Ω·cm^2, respectively, by least-squares linear fitting between −0.01 and 0.01 V. The n^+-Si//ITO/p^+-Si junctions showed the smallest interface resistance among all the junctions.

The *I–V* characteristics of p^+-Si//ITO/n^+-Si, n^+-Si//ITO/n^+-Si, and n^+-Si//ITO/p^+-Si junctions with annealing at different temperatures measured at room temperature are shown in Figs. 3(a)–3(c), respectively. It was found that the *I–V* characteristics of p^+-Si//ITO/n^+-Si, n^+-Si//ITO/n^+-Si, and n^+-Si//ITO/p^+-Si junctions without annealing revealed good linear properties and their *I–V* characteristics depended strongly on the annealing temperature. The interface resistances were found to be 0.029, 0.082, 0.146, and

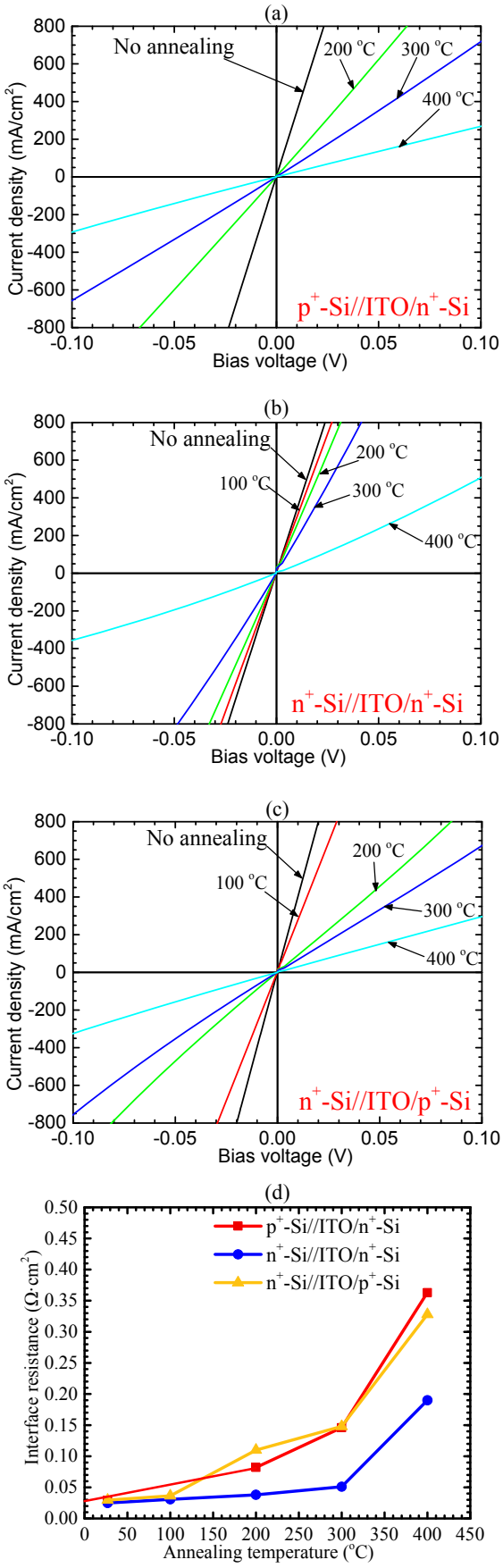

Fig. 3. (Color online) *I–V* characteristics of (a) p^+-Si//ITO/n^+-Si, (b) n^+-Si//ITO/n^+-Si, and (c) n^+-Si//ITO/p^+-Si junctions with annealing at different temperatures measured at room temperature and (d) interface resistances of p^+-Si//ITO/n^+-Si, n^+-Si//ITO/n^+-Si, and n^+-Si//ITO/p^+-Si junctions as a function of annealing temperature.

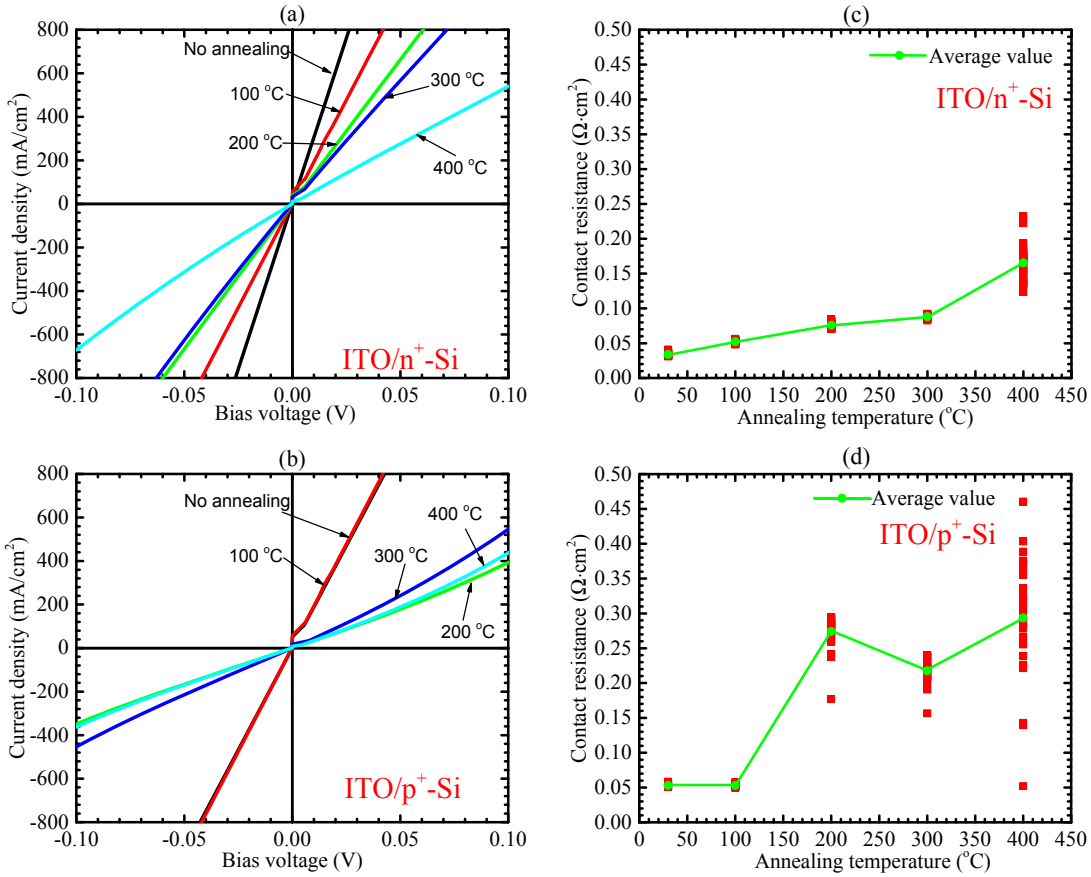

Fig. 4. (Color online) *I–V* characteristics of (a) ITO/n$^+$-Si and (b) ITO/p$^+$-Si junctions with annealing at different temperatures and contact resistances of (c) ITO/n$^+$-Si and (d) ITO/p$^+$-Si junctions as a function of annealing temperature. The solid line represents the average value of the contact resistances of 28 samples.

0.363 Ω·cm^2 for p$^+$-Si//ITO/n$^+$-Si junctions without and with annealing at 200, 300, and 400 °C, respectively, by least-squares linear fitting between −0.01 and 0.01 V. The resistances of n$^+$-Si//ITO/n$^+$-Si junctions without and with annealing at 100 and 200 °C and n$^+$-Si//ITO/p$^+$-Si junctions without and with annealing at 100 °C were obtained in similar manners. In addition, the resistances of n$^+$-Si//ITO/n$^+$-Si junctions with annealing at 300 and 400 °C and n$^+$-Si//ITO/p$^+$-Si junctions with annealing at 200, 300, and 400 °C were obtained by least-squares nonlinear fitting between −0.01 and 0.01 V because their *I–V* characteristics revealed nonlinear properties.

The obtained interface resistances as a function of annealing temperature are shown in Fig. 3(d). We found that the interface resistance increases with the annealing temperature increasing for all the junctions. The interface resistance of p$^+$-Si//ITO/n$^+$-Si junctions with annealing at respective temperatures is almost consistent with that of n$^+$-Si//ITO/p$^+$-Si junctions. The interface resistance of n$^+$-Si//ITO/n$^+$-Si junctions with annealing at higher than 100 °C was found to be the smallest among all the junctions. In addition, note that the interface resistance of n$^+$-Si//ITO/n$^+$-Si junctions increased gradually with increasing annealing temperature up to 300 °C, while annealing at temperatures above 300 °C caused a large increase in the interface resistance.

The *I–V* characteristics of ITO/n$^+$-Si and ITO/p$^+$-Si junctions with annealing at different temperatures are shown in Figs. 4(a) and 4(b), respectively. It was observed that the *I–V* characteristics of ITO/n$^+$-Si and ITO/p$^+$-Si junctions without and with annealing at 100 °C revealed a good linearity. Their *I–V* characteristics revealed nonlinear properties after the junctions were annealed at higher than 100 °C. The contact resistances of ITO/n$^+$-Si junctions were determined to be 0.0329, 0.0523, 0.0756, 0.0753, and 0.1423 Ω·cm^2 for the junctions without and with annealing at 100, 200, 300, and 400 °C, respectively, by least-squares linear fitting and nonlinear fitting between −0.01 and 0.01 V. By the same methods, we found that the contact resistances of ITO/p$^+$-Si junctions without and with annealing at 100, 200, 300, and 400 °C are 0.0533, 0.0524, 0.1568, 0.1182, and 0.1565 Ω·cm^2, respectively. It was found that the contact resistances of ITO/n$^+$-Si junctions with annealing at different temperatures are smaller than those of ITO/p$^+$-Si junctions.

The contact resistances of 28 samples of ITO/n$^+$-Si and ITO/p$^+$-Si junctions as a function of annealing temperature are shown in Figs. 4(c) and 4(d), respectively. The contact resistances of ITO/n$^+$-Si junctions with annealing temperature lower than 300 °C showed high uniformity, while with the annealing temperature as high as 400 °C, the dispersion of the resistance was observed. In contrast to ITO/n$^+$-Si junctions, no dispersion was observed in ITO/p$^+$-Si junctions with annealing at a temperature lower than 100 °C. The dispersion of the resistance was observed after the junctions were annealed at 200 °C. Furthermore, the dispersion was markedly enlarged with increasing annealing temperature. In addition, the contact resistances of ITO/n$^+$-Si and ITO/p$^+$-Si junctions increase with the increase in annealing temperature.

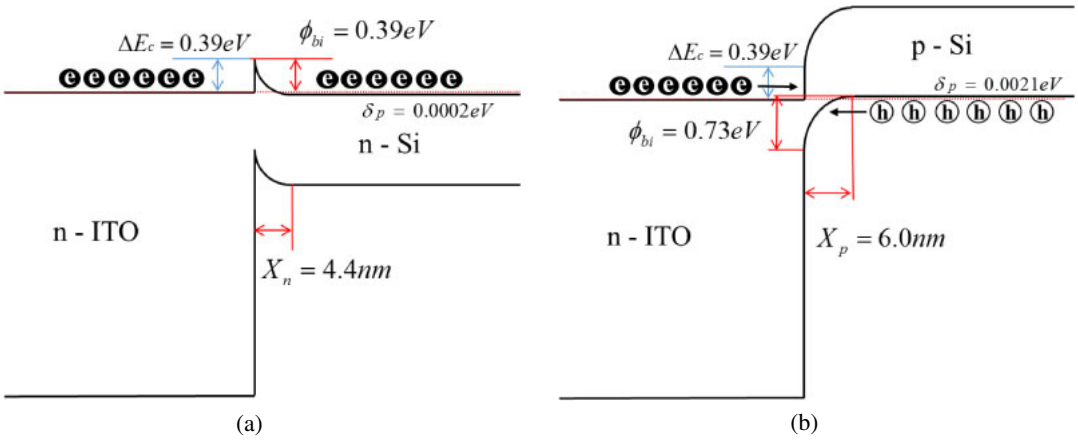

Fig. 5. (Color online) Schematic energy-band diagrams of (a) ITO/n^+-Si and (b) ITO/p^+-Si junctions.

4. Discussion

Note that the variation of the interface resistance in n^+-Si//ITO/n^+-Si junctions and p^+-Si//ITO/n^+-Si and n^+-Si//ITO/p^+-Si junctions with annealing at various temperatures is consistent with the annealing temperature dependence of the contact resistance in ITO/n^+-Si and ITO/p^+-Si junctions, respectively. Furthermore, the electrical conductivity of ITO/n^+-Si junctions is better than that of ITO/p^+-Si junctions. On the basis these results, we can conclude that the electrical conductivities of p^+-Si//ITO/n^+-Si and n^+-Si//ITO/p^+-Si junctions are dominated by the carrier transport properties of the ITO/p^+-Si interface, and the difference in the electrical conductivity between ITO/n^+-Si and ITO/p^+-Si junctions should be related to the electrical transport properties across the ITO/Si interfaces.

It was found that the *I–V* characteristics of a silicon Schottky diode should be observed in ITO/p^+-Si junctions, which is in contradiction with the experimental result. The main reason for the difference between the theoretical and experimental results should be attributed to the formation of the interface defects. It was reported that an interfacial amorphous layer of silicon oxide of 2–3 nm thickness was formed at the ITO/Si interface fabricated by the plasma-based deposition method.[27–29] The surface bombardment during the growth process was assumed to induce the interfacial amorphous layer, which is similar to the amorphous layer formed at the bonding interface by Ar atom fast beam irradiation during the SAB process.[14] The interface states were distributed in the amorphous layer. It is consequently assumed that the tunneling-assisted recombination via the interface states formed in the amorphous layer plays a major role in the transport properties of carriers across the ITO/Si interfaces.

The energy-band diagrams of the ITO/n^+-Si and ITO/p^+-Si junctions at zero bias voltage and room temperature are shown in Figs. 5(a) and 5(b), respectively. Note that these diagrams are based on the carrier concentrations of p^+-Si and n^+-Si substrates mentioned in experimental procedure and the assumption that there are no additional charges located at the interfaces. It is assumed that the Fermi level of ITO coincides with the conduction band edge, and the carrier concentration of ITO is much higher than those of p^+-Si and n^+-Si substrates. The conduction band offset between ITO and Si was reported to be 0.39 eV in the ITO/Si junctions fabricated by radio frequency sputtering.[20] The depletion layer should be formed predominantly on the Si side of the interface as expected from the Schottky–Mott model.[30] The width of the depletion layer (W_D) on the Si side of ITO/n^+-Si and ITO/p^+-Si junctions was calculated to be 4.4 and 6.0 nm, respectively, using the following formula:

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_s\phi_{bi}}{qN_{D(A)}}}. \quad (1)$$

Here, ε_0 and ε_s are vacuum permittivity and the dielectric constant of Si, respectively, $N_{D(A)}$ is the concentration of donors (acceptors) in n^+-Si (p^+-Si) substrates, and ϕ_{bi} is the built-in potential of ITO/n^+-Si and ITO/p^+-Si junctions, which is simply the difference between the work function of ITO and n^+-Si and p^+-Si. The width of the depletion layer is smaller in the ITO/n^+-Si junction than in the ITO/p^+-Si junction, which enables the carriers to more effectively tunnel across the depletion layer of ITO/n^+-Si junctions in comparison with that of ITO/p^+-Si junctions. Furthermore, the built-in potential of ITO/p^+-Si junctions is much larger than that of ITO/n^+-Si junctions. Hence, the carrier injection should be more effective in ITO/n^+-Si junctions than in ITO/p^+-Si junctions. These results are in agreement with the measurement results of the *I–V* characteristics in the ITO/Si junctions.

We found that the electrical conductivity in all the junctions significantly degraded with the increase in annealing temperature. However, it has been reported that the resistivity of the ITO films deposited on Si substrates markedly decreased with increasing annealing temperature.[31,32] The increase in electrical conductivity of the ITO film was attributed to the elimination of the positron traps such as vacancies and vacancy clusters around the grain boundaries and the improvement of ITO film crystallinity. It has also been reported that the thickness of the interfacial amorphous oxide layer formed at the ITO/Si interface increased as the annealing temperature increased.[27] Hence, we suggest that the degradation of the electrical conductivity in all the ITO/Si junctions with annealing at high temperature should contribute to the increase in the thickness of the interfacial amorphous oxide layer. Note that the interface resistances of p^+-Si//ITO/n^+-Si, n^+-Si//ITO/n^+-Si, and n^+-Si//ITO/p^+-Si junctions without annealing are smaller than

those of n^+-Si/p^+-Si and n^+-Si/n^+-Si junctions fabricated by SAB.[15] Furthermore, the interface resistances of Si/ITO/Si junctions are sufficiently low for application in concentrator photovoltaics.[33] These results indicated that ITO as an intermediate layer has great potential to reduce the resistance of the bonding interface.

5. Conclusions

n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions were fabricated by bonding ITO films deposited on Si substrates to Si substrates using SAB and their electrical properties were investigated by measuring *I–V* characteristics at room temperature. The *I–V* characteristics of all the junctions without annealing showed linear properties. The interface resistances of n^+-Si//ITO/n^+-Si, n^+-Si//ITO/p^+-Si, and p^+-Si//ITO/n^+-Si junctions without annealing were estimated to be 0.030, 0.025, and 0.029 $\Omega\cdot cm^2$, respectively. It is important that the interface resistances of all the Si/ITO/Si junctions without annealing are less than the required value for concentrator photovoltaics operation. Their electrical conductivities significantly degraded with increasing annealing temperature. The reason for the degradation of the electrical conductivity was correlated with the variation in the thickness of the interface amorphous oxide layer during annealing. The degradation level of the electrical conductivity in n^+-Si//ITO/n^+-Si junctions is the smallest among all the junctions. These results demonstrated that ITO as an intermediate layer could be used for connecting subcells in tandem solar cells fabricated by SAB.

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