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Determination of Band Structure at GaAs/4H-SiC Heterojunctions

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The effects of thermal annealing process on the interface in p+-GaAs/n-4H-SiC heterojunctions fabricated by using surface-activated bonding (SAB) were investigated. It was found by measuring their current-voltage (*I-V*) characteristics that the reverse-bias current and the ideality factor were extracted to be 7.57×10^{-7} A/cm^2 and 1.33, respectively, for the junctions annealed at 400 °C. The flat-band voltage obtained from capacitance-voltage (*C-V*) measurements was found to be 1.29 eV, which is almost consistent with the turn-on voltage extracted from *I-V* characteristics. These results suggest that the SAB-based GaAs/4H-SiC heterojunctions are applicable for fabricating high-frequency power devices.

Introduction

Heterojunctions are widely used for fabricating high performance electrical and optical device. The heterojunction fabricated by conventional epitaxial growth generally introduces a large number of crystalline defect densities at the interface due to the large differences in crystal lattice and thermal expansion coefficient (1, 2). To solve these difficulties a variety of wafer bonding methods have been employed to fabricate semiconductor hetero-structure. Among them the most effective candidate is surface activated bonding (SAB) (3-9). In this method, surfaces of substrates are activated by the irradiation of Ar fast atom beams prior to bonding and consequently bring into contact in a vacuum condition. It enables us to fabricate heterojunctions composed of dissimilar materials with large mismatched lattice constants. We previously fabricated p-Si/n-SiC and p-Si/n-GaAs heterojunctions and investigated their electrical properties (7, 10). It was found that the energy band diagram of p-Si/n-GaAs and p-Si/n-SiC junctions revealed type-II and type-I features, respectively. Furthermore, their conduction band discontinuities were calculated to be 0.59 and 0.3 eV, respectively. If SAB-based GaAs/SiC heterojunction are realized, the conduction band discontinuity of less than 0.3 eV should be expected, which should be suitable for fabricating devices with excellent high-frequency, high-temperature, and high-power performances that have not yet been achievable by each component material alone.

In this work, we fabricated p$^+$-GaAs/n-SiC heterojunction by using SAB method and have investigated the annealing temperature dependence of the band structure of GaAs/SiC heterojunction. The influence of the thermal annealing process on the electrical properties of the junctions were systematically investigated by measuring their current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics. The applicability of

GaAs/SiC heterojunctions for functional devices was explored based on these measurements.

Experiments

p^+-GaAs (100) epitaxial substrates (400 nm, ~ 1×10^{19} cm^{-3} epitaxial layer / substrate ~ 1×10^{18} cm^{-3}) and n-4H-SiC epitaxial substrates (2.8 μm, 1.1×10^{17} cm^{-3} epitaxial layer / 0.5 μm, > 2×10^{18} cm^{-3} buffer layer / substrate ~ 1×10^{19} cm^{-3}) were used for the bonding experiment. Before bonding Al/Ni/Au multilayers were evaporated on the backside of n-SiC substrates. The ohmic contacts of n-SiC substrates were formed by a rapid thermal annealing at 1000 °C for 60 s in N_2 gas ambient. p^+-GaAs epitaxial substrates and n-SiC epitaxial substrates were bonded to each other by using SAB (3, 6). After the bonding, AuZn/Ti/Au multilayers were evaporated on the bottom surfaces of p-GaAs substrates. The p^+-GaAs/n-SiC heterojunctions were annealed separately at 100, 200, 300, and 400 °C for 60 s in N_2 gas ambient. All the samples were diced into 4 mm^2 pieces. The characteristics of these samples were also investigated while the junction was unannealed. Their *I-V* and *C-V* characteristics were measured using an ADCMT 6242 Source Measurement Unit and an Agilent E4980A Precision Impedance Analyzer, respectively.

Results

The *I-V* characteristics measured at room temperature are shown in Fig. 1. The GaAs/SiC heterojunction diodes showed good rectification properties. The ideality factor (n) for the forward bias voltages between 0.3 and 0.5 V was extracted to be 1.31, 1.38, 1.33, 1.32, and 1.33 for the unannealed junction and the junctions annealed at 100, 200, 300, and 400 °C, respectively.

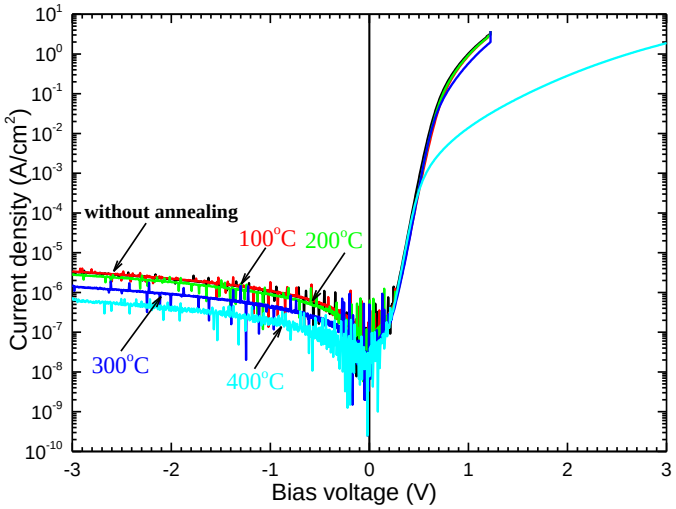

Figure. 1. *I-V* characteristics of p^+-GaAs/n-SiC heterojunctions without being annealed and annealed at 100, 200, 300, and 400 °C measured at room temperature.

It was found that the ideality factor (n) remained almost unaffected by the annealing temperature. In addition, the series resistance of the junctions was extracted from the slope of the measured *I-V* characteristics for the forward bias voltages between 0.8 and 1.2 V. We found that the resistance increased after annealing above 300 °C, which is attributed to the oxidation of the evaporated metal for the higher annealing process. In addition, the turn-on voltage of the junctions defined at the current of 100 mA/cm^2 dramatically increased from 0.73 to 1.55 V as the annealing temperature increased up to 400 °C. Moreover, the magnitude of the current increased as the junctions were more deeply reverse biased. Furthermore, as the annealing temperature increased, the magnitude of the reverse-bias current at - 3 V significantly decreased from 3.38×10^{-6} to 7.57×10^{-7} A/cm^2. The values of parameters for the respective junctions are summarized in Table I.

TABLE I. The reverse-bias current, turn-on voltage, ideality factor, resistance, and conduction-band offset of p$^+$-GaAs/n-SiC junctions.

Annealing temperature	Reverse-bias current (A/cm^2)	Turn-on voltage (V)	Ideality factor	Resistance (Ω·cm^2)	ΔE_c (eV)
Without annealing	3.38×10^{-6}	0.73	1.31	0.08	0.17
100 °C	3.44×10^{-6}	0.76	1.38	0.08	0.17
200 °C	2.82×10^{-6}	0.75	1.33	0.09	0.17
300 °C	1.51×10^{-6}	0.78	1.32	0.14	0.16
400 °C	7.57×10^{-7}	1.55	1.33	0.41	0

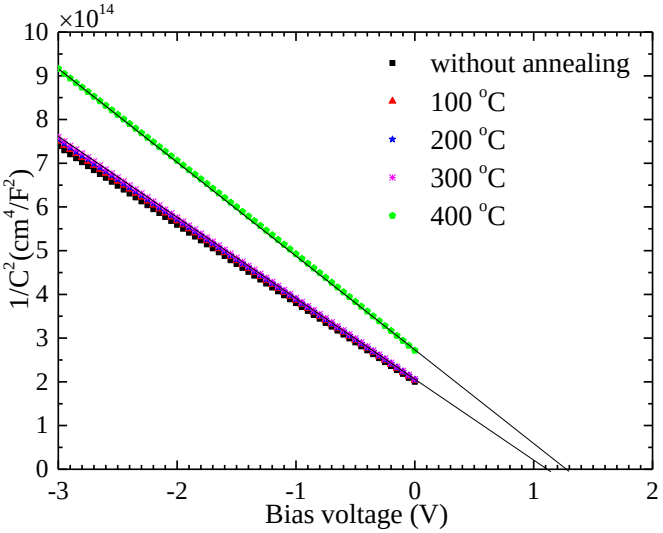

Figure 2. *C-V* characteristics of p$^+$-GaAs/n-SiC heterojunctions without being annealed and annealed at 100, 200, 300, and 400 °C measured at room temperature.

The *1/C^2-V* characteristics measured at room temperature and a frequency of 100 kHz are shown in Fig. 2. The characteristics indicated a straight line and the flat-band voltages (V_d) were found to be 1.12, 1.12, 1.12, 1.13 and 1.29 V for the unannealed junction and junctions annealed at 100, 200, 300, and 400 °C, respectively, by linearly extrapolating 1/C^2 to zero. It is noteworthy that the flat-band voltages remained constant as the annealing temperature increased up to 200 °C and then increased as the annealing temperature increased from 300 to 400 °C. Using the slopes of *1/C^2-V* characteristics, the

donor concentrations of the n-SiC epitaxial layer were estimated to be 8.14×10^{16}, 8.02×10^{16}, 7.98×10^{16}, 7.93×10^{16}, and 6.94×10^{16} cm^{-3}, for the unannealed junction and junctions annealed at 100, 200, 300, and 400 °C, respectively, which are close to the norminal value of 1.1 × 1017 cm^{-3}, as determined by Ni/n-SiC Schottky diode.

The *I-V* characteristics of the heterojunction annealed at 400 °C measured at various temperatures are shown in Fig. 3(a). The respective curves revealed a more marked asymmetric nature at lower temperature. Furthermore, as the temperature was raised, the magnitude of the current for the reverse bias voltages increased while their slope remained almost invariant to temperature. The dependence of the ideality factor and turn-on voltage as a function of temperatures in the range of 88 - 473 K are shown in Fig. 3(b). It can be seen that both parameters exhibited strong temperature dependence and the turn-on voltage decreased and the ideality factor increased with increasing the ambient temperature.

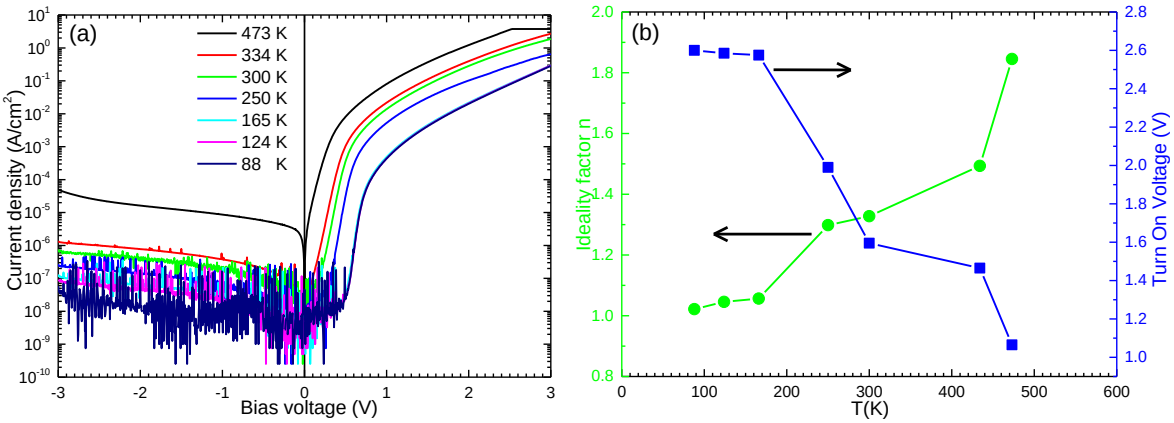

Figure 3. (a) *I-V* characteristics of p^+-GaAs/n-SiC heterojunctions annealed at 400 °C measured at various temperatures and (b) Temperature dependence of flat-band voltage and ideality factor (n) as function of temperatures in the range of 88 - 473 K.

Discussion

We observed that the turn-on voltage (~ 0.75 V) was smaller compared with the flat-band voltage (~ 1.2 V) and the magnitude of the current increased for larger reverse bias voltage for respective curves. Similar result was observed in the p-GaAs/n-GaN (11) and p-SiC/n-GaN (12) junctions fabricated by wafer fusion and molecular beam epitaxy, respectively, which was attributed to the scheme of interface states assisted tunneling. The interface states should be formed at the boding interface of the p^+-GaAs/n-SiC heterojunction and distributed in the amorphous layer of the bonded interface, which is due to damages fabricated during the Ar plasma irradiation in the SAB process according to our previous report. Furthermore, the 2.5 nm thick amorphous layer formed at the bonded interface was reported in the GaAs/SiC wafer bonded by SAB (13). If the electron transport property is dominated by carrier recombination or tunneling through the interface sates, the ideality factor should be close to 2. However, the extracted ideality factors (n) are as low as ~ 1.3 irrespective of the annealing condition.

Note that the linear extrapolation of $1/C^2$ is based on the assumption that no electric charges are placed at the GaAs/SiC interfaces. In this scheme, V_d is given by the difference in the work functions between p$^+$-GaAs and n-SiC and is expressed as

$$qV_d = E_{gp} - \Delta E_c - \delta_{n-SiC} - \delta_{p^+-GaAs} \quad (1)$$

where q is the elementary charge, is the energy gap of p$^+$-GaAs, is the conduction-band offset, and and refer to the position of the Fermi energies relative to the valence-band maximum in p$^+$-GaAs and that relative to the conduction-band minimum in n-SiC, respectively. Using eq. (1), the values of were determined for the unannealed junction and junctions annealed at 100, 200, 300, and 400 °C and are summarized in Table I. It is noteworthy that is ≈ 0 eV, which means that is ≈ 1.8 eV for heterojunctions annealed at 400 °C. The energy band diagrams of the heterojunction annealed at 400 °C based on the estimation is shown in Fig. 4(a). Their diagram suggests that minority electrons in p$^+$-GaAs layers could be transported into n-SiC layers without the inference of heterointerfaces, which means that the GaAs/SiC heterojunctions are suitable for fabrication of high frequency power devices (such as heterojunction bipolar transistors).

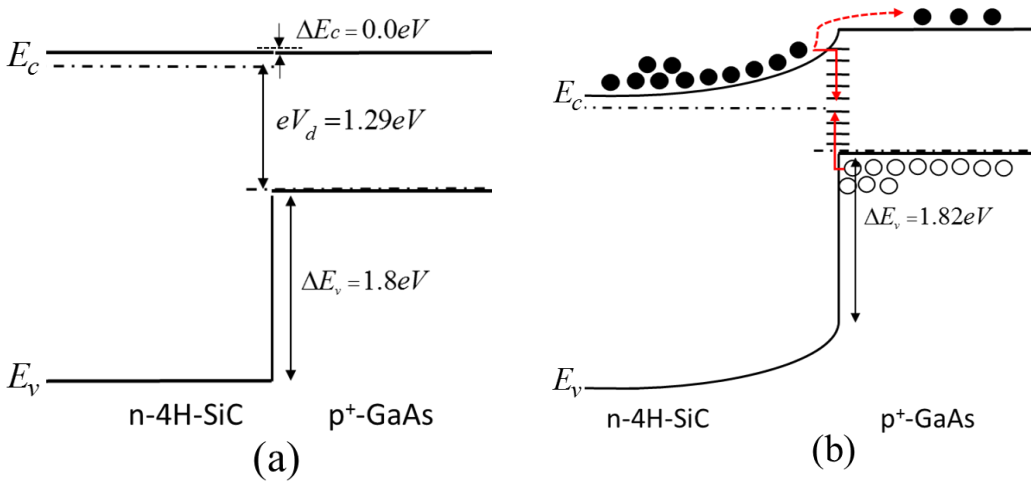

Figure 4. (a) Flat-band diagrams of p$^+$-GaAs/n-SiC heterojunctions and (b) Band diagrams of p$^+$-GaAs/n-SiC heterojunctions under the forward bias.

We have to note that the ideality factor continuously increased and the turn-on voltage decreased as the ambient temperature was raised, as shown in Fig. 3(b). This phenomenon can be explained on the basis of Fig. 4(b), where the band diagram of the GaAs/SiC heterojunction under the forward bias is shown. The electrons accumulated near the interface of the GaAs/SiC heterojunction drop into the interface states and recombine with the trapped holes. The rate of the capture of holes from the valence band increases with increasing temperature (14). The bias voltage and the temperature dependence of the reverse-bias current suggest that the electrons in the valence band edge of the p$^+$-GaAs were thermally excited to the interface states, and then tunnel into the conduction band of the n-SiC for the reverse bias. In addition, the activation energy was estimated to be 0.25 eV from the temperature dependence of the reverse-bias current.

The features in the p^+-GaAs/n-SiC heterojunction after annealing at 400 °C that (1) the reverse-bias current at – 3V decreased to 7.57×10^{-7} A/cm^2, (2) the obtained turn-on voltage is consistent with the flat-band voltage extracted from C-V measurement, and (3) the determined ideality factor (1.33) is close to 1 indicated that the impacts of the interface states on the conductive properties of the GaAs/SiC heterojunction is comparatively small and the diffusion current mechanism mainly dominates the transport properties of carriers across the interface. These results suggest that the SAB-based GaAs/SiC heterojunctions are expected to play a significant role for fabricating high-power and high-frequency devices.

Conclusion

The lattice-mismatched p^+-GaAs/n-SiC heterojunctions were realized by using the surface-activated bonding without heating. The influence of thermal annealing process on the interface of the p^+-GaAs/n-SiC heterojunctions was demonstrated. The reverse-bias current at – 3 V decreased with increasing the ambient temperature, the value was finally reduced to 7.57×10^{-7} A/cm^2 after annealing at 400 °C. The flat-band voltage extrapolated from the *C-V* characteristics, which is close to the turn-on voltage obtained from the *I-V* characteristics. The conduction-band offset extracted from the *C-V* characteristics was found to be 0 eV. This result suggested that the band profile of the GaAs/SiC heterojunction was likely to be preferable for fabricating collector junction in heterojunction bipolar transistors. Thus, the SAB technology in combination with the termal annealing is likely to be useful for fabricating devices for high-power applications.

Acknowledgements

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